10069402

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
NNEX0004P		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US 01/ 19792	20/06/2001	20/06/2000
Applicant		
NANONEXUS, INC.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [ ] the text is approved as submitted by the applicant.

   [X] the text has been established by this Authority to read as follows:

   SYSTEMS FOR TESTING INTERGRATED CIRCUITS DURING BURN-IN

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 21

   [ ] as suggested by the applicant.

   [X] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [ ] None of the figures.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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60/213,729 22 June 2000 (22.06.2000) US

(71) Applicant *(for all designated States except US)*: **NANONEXUS, INC.** [US/US]; 400 Kato Terrace, Fremont, CA 94539 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **MOK, Sammy** [CA/US]; 106360 E. Estates Drive, Cupertino, CA 95014 (US). **CHONG, Fu, Chiung** [MY/US]; 19743 Glen Brae Drive, Saratoga, CA 95070 (US).

(74) Agents: **GLENN, Michael** et al.; Glenn Patent Group, Suite L, 3475 Edison Way, Menlo Park, CA 94025 (US).

(81) Designated States *(national)*: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

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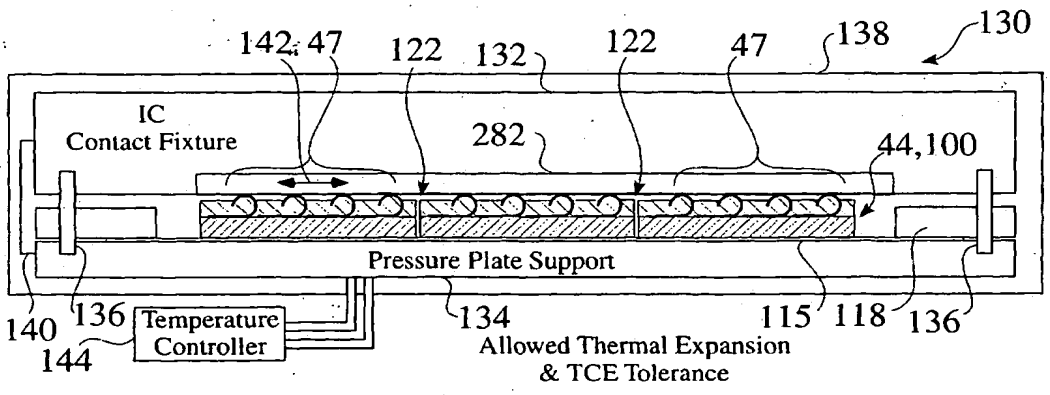
25 July 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SYSTEMS FOR TESTING INTEGRAGED CIRCUITS DURING BURN-IN



(57) Abstract: Several embodiments of stress metal springs are disclosed, which typically comprise a plurality of stress metal layers that are established on a substrate, which are then controllably patterned and partially released from the substrate. An effective rotation angle is typically created in the formed stress metal springs, defining a looped spring structure. The formed springs provide high pitch compliant electrical contacts for a wide variety of interconnection systems, including chip scale semiconductor packages, high density interposer connectors, and probe contactors. Several embodiments of massively parallel interface integrated circuit test assemblies are also disclosed, comprising one or more substrates having stress metal spring contacts, to establish connections between one or more separated integrated circuits on a compliant wafer carrier.

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INTERNATIONAL SEARCH REPORT

International Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G01R1/073 G01R3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G01R H01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	WO 99 18445 A (NEW JERSEY TECH INST) 15 April 1999 (1999-04-15) abstract	23-25 86,106
X	US 5 944 537 A (THORNTON ROBERT L ET AL) 31 August 1999 (1999-08-31) abstract	23,24
Y	US 5 756 021 A (SHIH DA-YUAN ET AL) 26 May 1998 (1998-05-26) figure 5	23,24
Y	US 5 385 477 A (VAYNKOF YAKOV F ET AL) 31 January 1995 (1995-01-31) abstract	23,25

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 February 2002	20/02/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Vytlacilová, L

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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A	figures 10-13	1,4-6, 22,52
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A	US 3 842 189 A (SOUTHGATE P) 15 October 1974 (1974-10-15) claims 1-5	23
Y	US 5 801 441 A (SMITH JOHN W ET AL) 1 September 1998 (1998-09-01) figure 22	67,69
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(74) Agents: **GLENN, Michael** et al.; Glenn Patent Group, Suite L., 3475 Edison Way, Menlo Park, CA 94025 (US).

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(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

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WO 01/98793 A2

(54) Title: SYSTEMS FOR TESTING AND PACKAGING INTEGRAGED CIRCUITS

(57) Abstract: Several embodiments of stress metal springs are disclosed, which typically comprise a plurality of stress metal layers that are established on a substrate, which are then controllably patterned and partially released from the substrate. An effective rotation angle is typically created in the formed stress metal springs, defining a looped spring structure. The formed springs provide high pitch compliant electrical contacts for a wide variety of interconnection systems, including chip scale semiconductor packages, high density interposer connectors, and probe contactors. Several embodiments of massively parallel interface integrated circuit test assemblies are also disclosed, comprising one or more substrates having stress metal spring contacts, to establish connections between one or more separated integrated circuits on a compliant wafer carrier.

Systems for Testing and Packaging Integrated Circuits

FIELD OF THE INVENTION

The invention relates to the field of integrated circuit (IC) package and wafer design, as well as to the fields of interconnection, testing and burn-in structures and processes. More particularly, the invention relates to improvements in photolithography-patterned spring contacts and enhanced system interconnect assemblies having photolithography-patterned spring contacts for use in the testing or burn-in of integrated circuits, and for interconnecting a large number of signals between electronic systems or subsystems.

BACKGROUND OF THE INVENTION

Integrated circuits are typically tested in wafer form (wafer sort) before they are packaged. During wafer sort, integrated circuits are tested one or few at a time, even though there may be hundreds or even thousands of the same integrated circuit located on a wafer. The packaged integrated circuits are then tested again, and burned-in, if necessary.

Prior to dicing the integrated circuits into individual dice on the wafer, the integrated circuits are placed (built) precisely on the wafer, but after dicing and separating the integrated circuits into individual dice for packaging and test, the packaged dices are handled individually, loosing the parallelism in handling.

Parallel testing on the wafer level has been limited in number and has so far been limited to low pin count devices, due to the difficulty in managing the large number of interconnects, and the limited amount of electronics which can conventionally be placed close to a wafer under test.

Attempts have also been made to burn-in ICs while in the wafer form. However, wafer-level burn-in is plagued with multiple problems, such as thermal expansion mismatch between the connector and the silicon wafer under test. Conventional structures, such as large area substrates having a large plurality of fanout traces which are electrically connected to pin or socket connectors, are typically implemented to manage connections between the IC under test, test electronics, and power management electronics.

The density of integrated circuits on semiconductor wafers continues to increase, due to semiconductor device scaling, with more gates and memory bits per unit area of silicon. As well, the use of larger semiconductor wafers (*e.g.* often having a nominal diameter of 8 inches or 12 inches) has become common. However, semiconductor test costs have increased on a cost per unit area of silicon basis. Therefore, semiconductor test costs have increased disproportionately over time, to become a greater percentage of the total manufacturing cost for each integrated circuit device.

Furthermore, advances in chip scale packaging (CSP) and other forms of small footprint packages have often made traditional packaged IC handlers obsolete for testing and burn-in.

In some conventional large surface area substrate integrated circuit (IC) test boards, electrical contacts between the test board and an integrated circuit wafer are typically provided by tungsten needle probes. However, tungsten needle probe technology is not able to meet the interconnect requirements of advanced semiconductors having higher pin counts, smaller pad pitches, and higher clock frequencies.

While emerging technologies have provided spring probes for different probing applications, most probes have inherent limitations, such as limited pitch, limited pin count, varying levels of flexibility, limited probe tip geometries, limitations of materials, and/or high costs of fabrication.

K. Banerji, A. Suppelsa, and W. Mullen III, *Selectively Releasing Conductive Runner and Substrate Assembly Having Non-Planar Areas,* U.S. Patent No. 5,166,774 (24 November 1992) disclose a runner and substrate assembly which comprises "a plurality of conductive runners adhered to a substrate, a portion of at least some of the conductive runners have non-planar areas with the substrate for selectively releasing the conductive runner from the substrate when subjected to a predetermined stress".

A. Suppelsa, W. Mullen III and G. Urbish, *Selectively Releasing Conductive Runner and Substrate Assembly,* U.S. Patent No. 5,280,139 (18 January 1994) disclose a runner and substrate assembly which comprises "a plurality of conductive runners adhered to a substrate, a portion of at least some of the conductive runners have a lower adhesion to the substrate for selectively releasing the conductive runner from the substrate when subjected to a predetermined stress".

D. Pedder, *Bare Die Testing,* U.S. Patent No. 5,786,701 (28 July 1998) disclose a testing apparatus for testing integrated circuits (ICs) at the bare die stage, which includes

"a testing station at which microbumps of conductive material are located on interconnection trace terminations of a multilayer interconnection structure, these terminations being distributed in a pattern corresponding to the pattern of contact pads on the die to be tested. To facilitate testing of the die before separation from a wafer using the microbumps, the other connections provided to and from the interconnection structure have a low profile".

D. Grabbe, I. Korsunsky and R. Ringler, *Surface Mount Electrical Connector,* U.S. Patent No. 5,152,695 (06 October 1992) disclose a connector for electrically connecting a circuit between electronic devices, in which "the connector includes a platform with cantilevered spring arms extending obliquely outwardly therefrom. The spring arms include raised contact surfaces and in one embodiment, the geometry of the arms provide compound wipe during deflection".

H. Iwasaki, H. Matsunaga, and T. Ohkubo, *Partly Replaceable Device for Testing a Multi-Contact Integrated Circuit Chip Package,* U.S. Patent No. 5,847,572 (08 December 1998) disclose "a test device for testing an integrated circuit (IC) chip having side edge portions each provided with a set of lead pins. The test device comprises a socket base, contact units each including a contact support member and socket contact numbers, and anisotropic conductive sheet assemblies each including an elastic insulation sheet and conductive members. The anisotropic conductive sheet assemblies are arranged to hold each conductive member in contact with one of the socket contact members of the contact units. The test device further comprises a contact retainer detachably mounted on the socket base to bring the socket contact members into contact with the anisotropic sheet assemblies to establish electrical communication between the socket contact members and the conductive members of the anisotropic conductive sheet assemblies. Each of the contact units can be replaced by a new contact unit if the socket contact members partly become fatigued, thereby making it possible to facilitate the maintenance of the test device. Furthermore, the lead pins of the IC chip can be electrically connected to a test circuit board with the shortest paths formed by part of the socket contact members and the conductive members of the anisotropic conductive sheet assemblies".

W. Berg, *Method of Mounting a Substrate Structure to a Circuit Board,* U.S. Patent No. 4,758,9278 (19 July 1988) discloses "a substrate structure having contact pads is mounted to a circuit board which has pads of conductive material exposed at one main face of the board and has registration features which are in predetermined positions relative to the contact pads of the circuit board. The substrate structure is provided with leads which are electrically connected to the contact pads of the substrate structure and

project from the substrate structure in cantilever fashion. A registration element has a plate portion and also has registration features which are distributed about the plate portion and are engageable with the registration features of the circuit board, and when so engaged, maintain the registration element against movement parallel to the general plane of the circuit board. The substrate structure is attached to the plate portion of the registration element so that the leads are in predetermined position relative to the registration features of the circuit board, and in this position of the registration element the leads of the substrate structure overlie the contact pads of the circuit board. A clamp member maintains the leads in electrically conductive pressure contact with the contact pads of the circuit board".

D. Sarma, P. Palanisamy, J. Heam and D. Schwarz, *Controlled Adhesion Conductor,* U.S. Patent No. 5,121,298 (09 June 1992) disclose "Compositions useful for printing controllable adhesion conductive patterns on a printed circuit board include finely divided copper powder, a screening agent and a binder. The binder is designed to provide controllable adhesion of the copper layer formed after sintering to the substrate, so that the layer can lift off the substrate in response to thermal stress. Additionally, the binder serves to promote good cohesion between the copper particles to provide good mechanical strength to the copper layer so that it can tolerate lift off without fracture".

R. Mueller, *Thin-Film Electrothermal Device,* U.S. Patent No. 4,423,401 (27 December 1983) discloses " A thin film multilayer technology is used to build micro miniature electromechanical switches having low resistance metal-to-metal contacts and distinct on-off characteristics. The switches, which are electrothermally activated, are fabricated on conventional hybrid circuit substrates using processes compatible with those employed to produce thin-film circuits. In a preferred form, such a switch includes a cantilever actuator member comprising a resiliently bendable strip of a hard insulating material (*e.g.* silicon nitride) to which a metal (*e.g.* nickel) heating element is bonded. The free end of the cantilever member carries a metal contact, which is moved onto (or out of) engagement with an underlying fixed contact by controlled bending of the member via electrical current applied to the heating element".

S. Ibrahim and J. Elsner, *Multi-Layer Ceramic Package,* U.S. Patent No. 4,320,438 (16 March 1982) disclose "In a multi-layer package, a plurality of ceramic lamina each has a conductive pattern, and there is an internal cavity of the package within which is bonded a chip or a plurality of chips interconnected to form a chip array. The chip or chip array is connected through short wire bonds at varying lamina levels to metallized conductive patterns thereon, each lamina level having a particular conductive pattern. The conductive patterns on the respective lamina layers are interconnected either by

tunneled through openings filled with metallized material, or by edge formed metallizations so that the conductive patterns ultimately connect to a number of pads at the undersurface of the ceramic package mounted onto a metalized board. There is achieved a high component density; but because connecting leads are "staggered" or connected at altemating points with wholly different package levels, it is possible to maintain a 10 mil spacing and 10 mil size of the wire bond lands. As a result, there is even greater component density but without interference of wire bonds one with the other, this factor of interference being the previous limiting factor in achieving high component density networks in a multi layer ceramic package".

F. McQuade, and J. Lander, *Probe Assembly for Testing Integrated Circuits,* U.S. Patent No. 5,416,429 (16 May 1995) disclose a probe assembly for testing an integrated circuit, which "includes a probe card of insulating material with a central opening, a rectangular frame with a smaller opening attached to the probe card, four separate probe wings each comprising a flexible laminated member having a conductive ground plane sheet, an adhesive dielectric film adhered to the ground plane, and probe wing traces of spring alloy copper on the dielectric film. Each probe wing has a cantilevered leaf spring portion extending into the central opening and terminates in a group of aligned individual probe fingers provided by respective terminating ends of said probe wing traces. The probe fingers have tips disposed substantially along a straight line and are spaced to correspond to the spacing of respective contact pads along the edge of an IC being tested. Four spring clamps each have a cantilevered portion which contact the leaf spring portion of a respective probe wing, so as to provide an adjustable restraint for one of the leaf spring portions. There are four separate spring clamp adjusting means for separately adjusting the pressure restraints exercised by each of the spring clamps on its respective probe wing. The separate spring clamp adjusting means comprise spring biased platforms each attached to the frame member by three screws and spring washers so that the spring clamps may be moved and oriented in any desired direction to achieve alignment of the position of the probe finger tips on each probe wing".

D. Pedder, *Structure for Testing Bare Integrated Circuit Devices,* European Patent Application No. EP 0 731 369 A2 (Filed 14 February 1996), U.S. Patent No. 5,764,070 (09 June 1998) discloses a test probe structure for making connections to a bare IC or a wafer to be tested, which comprises "a multilayer printed circuit probe arm which carries at its tip an MCM-D type substrate having a row of microbumps on its underside to make the required connections. The probe arm is supported at a shallow angle to the surface of the device or wafer, and the MCM-D type substrate is formed

with the necessary passive components to interface with the device under test. Four such probe arms may be provided, one on each side of the device under test".

B. Eldridge, G. Grube, I. Khandros, and G. Mathieu, *Method of Mounting Resilient Contact Structure to Semiconductor Devices,* U.S. Patent No. 5,829,128 (03 November 1998), *Method of Making Temporary Connections Between Electronic Components,* U.S. Patent No. 5,832,601 (10 November 1998), *Method of Making Contact Tip Structures,* U.S. Patent No. 5,864,946 (02 February 1999), *Mounting Spring Elements on Semiconductor Devices,* U.S. Patent No. 5,884,398 (23 March 1999), *Method of Burning-In Semiconductor Devices,* U.S. Patent No. 5,878,486 (09 March 1999), and *Method of Exercising Semiconductor Devices,* U.S. Patent No. 5,897,326 (27 April 1999), disclose "Resilient contact structures are mounted directly to bond pads on semiconductor dies, prior to the dies being singulated (separated) from a semiconductor wafer. This enables the semiconductor dies to be exercised (*e.g.* tested and/or burned-in) by connecting to the semiconductor dies with a circuit board or the like having a plurality of terminals disposed on a surface thereof. Subsequently, the semiconductor dies may be singulated from the semiconductor wafer, whereupon the same resilient contact structures can be used to effect interconnections between the semiconductor dies and other electronic components (such a wiring substrates, semiconductor packages, etc.). Using the all-metallic composite interconnection elements of the present invention as the resilient contact structures, burn-in can be performed at temperatures of at least 150° C., and can be completed in less than 60 minutes". While the contact tip structures disclosed by B. Eldridge et al. provide resilient contact structures, the structures are each individually mounted onto bond pads on semiconductor dies, requiring complex and costly fabrication. As well, the contact tip structures are fabricated from wire, which often limits the resulting geometry for the tips of the contacts. Furthermore, such contact tip structures have not been able to meet the needs of small pitch applications (*e.g.* typically on the order of 50 µm spacing for a peripheral probe card, or on the order of 75 µm spacing for an area array).

T. Dozier II, B. Eldridge, G. Grube, I. Khandros, and G. Mathieu, *Sockets for Electronic Components and Methods of Connecting to Electronic Components,* U.S. Patent No. 5,772,451 (30 June 1998) disclose "Surface-mount, solder-down sockets permit electronic components such as semiconductor packages to be releaseably mounted to a circuit board. Resilient contact structures extend from a top surface of a support substrate, and solder-ball (or other suitable) contact structures are disposed on a bottom surface of the support substrate. Composite interconnection elements are used as the resilient contact structures disposed atop the support substrate. In any suitable manner, selected ones of the resilient contact structures atop the support substrate are

connected, via the support substrate, to corresponding ones of the contact structures on the bottom surface of the support substrate. In an embodiment intended to receive an LGA-type semiconductor package, pressure contact is made between the resilient contact structures and external connection points of the semiconductor package with a contact force which is generally normal to the top surface of the support substrate. In an embodiment intended to receive a BGA-type semiconductor package, pressure contact is made between the resilient contact structures and external connection points of the semiconductor package with a contact force which is generally parallel to the top surface of the support substrate".

Other emerging technologies have disclosed probe tips on springs which are fabricated in batch mode processes, such as by thin-film or micro-electronic mechanical system (MEMS) processes.

D. Smith and S. Alimonda, *Photolithographically Patterned Spring Contact,* U.S. Patent No. 5,613,861 (25 March 1997), U.S. Patent No. 5,848,685 (15 December 1998), and International Patent Application No. PCT/US 96/08018 (Filed 30 May 1996), disclose a photolithography patterned spring contact, which is "formed on a substrate and electrically connects contact pads on two devices. The spring contact also compensates for thermal and mechanical variations and other environmental factors. An inherent stress gradient in the spring contact causes a free portion of the spring to bend up and away from the substrate. An anchor portion remains fixed to the substrate and is electrically connected to a first contact pad on the substrate. The spring contact is made of an elastic material and the free portion compliantly contacts a second contact pad, thereby contacting the two contact pads". While the photolithography patterned springs, as disclosed by Smith et al., are capable of satisfying many IC probing needs, the springs are small, and provide little vertical compliance to handle the planarity compliance needed in the reliable operation of many current IC prober systems. Vertical compliance for many probing systems is typically on the order of 0.004" - 0.010", which often requires the use of tungsten needle probes.

While interposers have been used as an interconnecting structure, conventional interposers have been limited by pitch density, as well as by long term reliability over elevated temperatures, such as commonly seen in test or burn-in environments.

While probe substrates have been used as an interconnecting structure, such as for probing solder bumped wafers, the conventional probe substrates are often expensive, and/or require long lead times. Vertical probes, such as the Cobra Probe™, are currently available from International Business Machines, of San Jose, CA. A

Microspring™ probe assembly is currently available from Form Factor, Inc., of Livermore CA.

T. Distefano, J. Smith and A. Faraci, *Fixtures and Methods for Lead Bonding and Deformation*, U.S. Patent No. 6,080,603 (27 June 2000), disclose "In a method for mounting a sheet-like microelectronic element, the sheet-like element comprises a dielectric layer having a top surface and a bottom surface and is first bonded to an expansion ring. The expansion ring is then heated to stretch the sheet-like element. A frame ring, having an external diameter smaller than the internal diameter of the expansion ring, is then bonded to the sheet-like element. A plurality of leads are formed on the bottom surface of the sheet-like element, the leads including bonding pads. In other embodiments, a method is provided for bonding bond pads on a sheet-like microelectronic element to contacts on a microelectronic component."

T. Distefano and J. Smith, *Methods of Making Connections to a Microelectronic Unit*, U.S. Patent No. 6, 044,548 (04 April 2000) disclose "A method of making connections to a microelectronic unit includes the steps of providing a connection component having a flexible dielectric top sheet, a plurality of terminals on the top sheet and a plurality of electrically conductive, elongated flexible leads connected to the terminals and extending side-by-side downwardly from the terminals away from the top sheet to bottom ends remote from the top sheet. The connection component is then engaged with a front surface of a microelectronic unit having an array of contacts thereon while subjecting the connection component and the microelectronic unit to heat and pressure so that bottom ends of the leads remote from the top sheet bond with the contacts on the microelectronic unit to form electrical connections therewith."

M. Beroz, B. Haba and C. Pickett, *Lead Formation Using Grids*, U.S. Patent No. 6,063,648 (16 May 2000) disclose "A component for making microelectronic units includes a grid of interspersed leads with ends of the various leads being connected to one another by frangible elements. One end of each lead is bonded to a top element and the other end of each lead is bonded to a bottom element. The top and bottom elements are moved away from one another, thereby breaking the frangible elements and deforming the leads towards a vertically extensive disposition. A flowable composition such as dielectric material may be injected around the leads during or after the moving step. The resulting unit may be used to form permanent or temporary connections between microelectronic elements."

K. Gilleo, G. Grube and G. Mathieu, *Compliant Semiconductor Chip Assemblies and Methods of Making Same*, U.S. Patent No. 6,020,220 (01 February 2000) disclose "A

semiconductor chip package assembly is mounted to contact pads on a die. A compliant interposer layer is disposed between the die and a dielectric substrate wiring layer. The contacts on the die are connected to terminals on the compliant interposer layer by means of a compliant, conductive polymer extending through apertures in the interposer layer. Compliancy in the interposer layer and in the conductive polymer permits relative movement of the terminals on the dielectric substrate wiring layer to the contacts on the die and hence relieves the shear forces caused by differential thermal expansion. The arrangement provides a compact packaged structure similar to that achieved through flip-chip bonding, but with markedly increased resistance to thermal cycling damage. Further, the packaged structure allows the standardization of the packages such that several companies can make competing chips that are packaged such that the resultant packaged structures are roughly the same as far as the end user is concerned."

T. DiStefano, Z. Kovac and J. Smith, *Bondable Compliant Pads for Packaging of a Semiconductor Chip and Method Therefor*, U.S. Patent No. 6,030,856 (29 February 2000) disclose "A method of making a microelectronic package includes providing first and second microelectronic elements having electrically conductive parts and disposing a resilient element having one or more intermediary layers capable of being wetted by an adhesive between the microelectronic elements. The resilient element includes fibrous material, a fibrous matrix and/or voids formed at the intermediary layers thereof. An adhesive is provided between the intermediary layers and the microelectronic elements. The adhesive is then cured while it remains in contact with the intermediary layers for bonding the resilient element and the microelectronic elements. The electrically conductive parts are then bonded together to form electrical interconnections. A microelectronic package comprising a resilient element including one or more intermediary layers capable of being wetted by an adhesive is also provided."

P. Bellaar, T. DiStefano, J. Fjelstad, C. Pickett and J. Smith, *Microelectronic Component with Rigid Interposer*, U.S. Patent No. 6,002,168 (14 December 1999) disclose "A microelectronic component for mounting a rigid substrate, such as a hybrid circuit to a rigid support substrate, such as a printed circuit board. The microelectronic component includes a rigid interposer which may have a chip mounted on its first surface; a pattern of contacts on the rigid interposer; a flexible interposer overlying the second surface of the rigid interposer; a pattern of terminals on the flexible interposer; flexible leads; and solder coated copper balls mounted on the flexible interposer. The microelectronic component may have a socket assembly mounted on the first surface of the rigid interposer. The microelectronic component may be mounted on a rigid support substrate."

B. Eldridge, G. Grube, I. Khandros and G. Mathieu, *Method of Making Contact Tip Structures*, U.S. Patent No. 5, 864,946 (02 February 1999) disclose "Resilient contact structures are mounted directly to bond pads on semiconductor dies, prior to the dies being singulated (separated) from a semiconductor wafer. This enables the semiconductor dies to be exercised (e.g., tested and/or burned-in) by connecting to the semiconductor dies with a circuit board or the like having a plurality of terminals disposed on a surface thereof. Subsequently, the semiconductor dies may be singulated from the semiconductor wafer, whereupon the same resilient contact structures can be used to effect interconnections between the semiconductor dies and other electronic components (such as wiring substrates, semiconductor packages, etc.). Using the all-metallic composite interconnection elements of the present invention as the resilient contact structures, burn-in can be performed at temperatures of at least 150° C., and can be completed in less than 60 minutes."

B. Eldridge, G. Grube, I. Khandros and G. Mathieu, *Wafer-Level Test and Burn-In, and Semiconductor Process*, U.S. Patent No. 6,032,356, disclose "Resilient contact structures are mounted directly to bond pads on semiconductor dies, prior to the dies being singulated (separated) from a semiconductor wafer. This enables the semiconductor dies to be exercised (e.g., tested and/or burned-in) in) by connecting to the semiconductor dies with a circuit board or the like having a plurality of terminals disposed on a surface thereof. Subsequently, the semiconductor dies may be singulated from the semiconductor wafer, whereupon the same resilient contact structures can be used to effect interconnections between the semiconductor dies and other electronic components (such as wiring substrates, semiconductor packages, etc.). Using the all-metallic composite interconnection elements of the present invention as the resilient contact structures, burn-in can be performed at temperatures of at least 150° C., and can be completed in less than 60 minutes."

D. Hembree, W. Farnworth and J. Wark, *Force Applying Probe Card and Test System for Semiconductor Wafers*, U.S. Patent No. 6,078,186 (20 June 2000) disclose "A probe card for testing a semiconductor wafer, a test method, and a test system employing the probe card are provided. The probe card includes: a substrate; an interconnect slidably mounted to the substrate; and a force applying mechanism for biasing contacts on the interconnect into electrical engagement with contacts on the wafer. The force applying mechanism includes spring loaded electrical connectors that provide electrical paths to the interconnect, and generate a biasing force. The biasing force is controlled by selecting a spring constant of the electrical connectors, and an amount of Z-

direction overdrive between the probe card and wafer. The probe card also includes a leveling mechanism for leveling the interconnect with respect to the wafer."

It would be advantageous to provide a chip scale package structure which comprises compliant electrical interconnections which can be built directly on the integrated circuit wafer without additional packaging steps, and is compatible with current IC processing lines. It would also be advantageous to provide an interposer structure having compliant high density electrical interconnections which can be manufactured using batch processes. Furthermore, it would be advantageous to provide a probe contactor structure having compliant high density electrical interconnections at lower force than conventional interposer techniques, which can be manufactured using batch processes.

The round trip transit time between a device under test and conventional test equipment is often longer then the stimulus to response times of high speed electronic circuits. It would be advantageous to provide a test interface system which reduces this transit time, by placing high speed test electronics in close proximity of the device under test, while meeting space and cost constraints. Furthermore, it would be advantageous to provide a test interface system which minimizes the cost, complexity, tooling, and tum around time required to change the test structure for the testing of different devices. The development of such a system would constitute a major technological advance.

It would be advantageous to provide a test interface system which provides probe contact with many, hundreds, or even hundreds of thousands of pads for one or more separated devices which are mounted on a compliant wafer carrier, such as for massively parallel testing and/or burn-in applications, wherein the pads may be in close proximity of one another, with a minimum spacing approaching 1 mil or less, while providing a uniform force and minimizing pad damage over the entire wafer. It would also be advantageous to provide such a test interface system which organizes and manages the interconnections between the devices under test and the tester electronics, while maintaining signal integrity and power and ground stability, and assures that no two or more adjacent pads are contacted by a single test probe tip. Furthermore, it would be advantageous to provide such a test structure which preferably provides planarity compliance with the devices under test. The development of such a system would constitute a further technological advance.

In addition, it would be advantageous to provide such a test system which preferably provides continuous contact with many, hundreds, or even hundreds of thousands of pads for one or more devices on a compliant wafer carrier over a wide temperature range, while providing thermal isolation between the test electronics and the devices

under test. As well, it would be advantageous to provide a system for separate thermal control of the test system and of the devices under test.

It would also be advantageous to provide a test interface system which may be used to detect power to ground shorts in any die quickly, and to isolate power from a die having a detected power to ground short, before damage is done to the test electronics. In addition, it would be advantageous to provide a test interface structure which can detect that the contacts to many, hundreds, or even hundreds of thousands of pads are reliably made and are each of the contacts are within the contact resistance specification, to assure that the self inductance and self capacitance of each signal line are below values that would adversely affect test signal integrity, and to assure that the mutual inductance and mutual capacitance between pairs of signal lines and between signal lines and power or ground lines are below values that would adversely affect test signal integrity. As well, it would also be advantageous to provide a test interface structure which provides stimulus and response detection and analysis to many, hundreds, or even thousands of die under test in parallel, and which preferably provides diagnostic tests to a failed die, in parallel with the continued testing of all other die.

Furthermore, it would be advantageous to provide a large array interface system which can reliably and repeatedly establish contact to many, hundreds, or even hundreds of thousands of pads, without the need to periodically stop and inspect and/or clean the probe interface structure.

It would also be advantageous to provide a system for massively parallel interconnections between electrical components, such as between computer systems, which utilize spring probes within the interconnection structure, to provide high pin counts, small pitches, cost-effective fabrication, and customizable spring tips. The development of such a method and apparatus would constitute a major technological advance.

SUMMARY OF THE INVENTION

Several embodiments of stress metal springs are disclosed, which typically comprise a plurality of stress metal layers that are established on a substrate, which are then controllably patterned and partially released from the substrate. An effective rotation angle is typically created in the formed stress metal springs, defining a looped spring structure. The formed springs provide high pitch compliant electrical contacts for a wide variety of interconnection structures, including chip scale semiconductor packages, high density interposer connectors, and probe contactors. Several embodiments of massively parallel interface integrated circuit test assemblies are also disclosed,

comprising one or more substrates having stress metal spring contacts, to establish connections between one or more separated integrated circuits on a compliant wafer carrier, and use one or more test modules which are electrically connected to the integrated circuits on the compliant wafer carrier through the substrates. The massively parallel interface assemblies provide tight pad pitch and compliance, and preferably enable the parallel testing or burn-in of multiple ICs. In some preferred embodiments, the massively parallel interface assembly structures include separable standard electrical connector components, which reduces assembly manufacturing cost and manufacturing time. These massively parallel interface structures and assemblies enable high speed testing of separated integrated circuit devices affixed to a compliant carrier, and allow test electronics to be located in close proximity to the integrated circuit devices under test. Preferred embodiments of the massively parallel interface assemblies provide thermal expansion matching to the wafer under test, and provide a thermal path for system electronic. Alternate massively parallel interface structures provide massively parallel connection interfaces, which may be used in a wide variety of circuitry, such as for interconnecting computers in a network, or for interconnecting other electronic circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a plan view of a linear array of photolithographically patterned springs, prior to release from a substrate;

Figure 2 is a perspective view of a linear array of photolithographically patterned springs, after release from a substrate;

Figure 3 is a side view of a first, short length photolithographically patterned spring, having a first effective radius and height after the short length spring is released from a substrate;

Figure 4 is a side view of a second, long length photolithographically patterned spring, having a second large effective radius and height after the long length spring is released from a substrate;

Figure 5 is a perspective view of opposing photolithographic springs, having an interleaved spring tip pattern, before the springs are released from a substrate;

Figure 6 is a perspective view of opposing photolithographic springs, having an interleaved spring tip pattern, after the springs are released from a substrate;

Figure 7 is a top view of a first opposing pair of interleaved multiple-point photolithographic spring probes, in contact with a single trace on an integrated circuit device, and a second opposing pair of interleaved multiple-point photolithographic spring probes, in contact with a single pad on the integrated circuit device;

Figure 8 is a plan view of opposing single-point photolithographic spring probes, before the springs are released from a substrate;

Figure 9 is a top view of parallel and opposing single-point photolithographic spring probes, after the springs are released from a substrate, in contact with a single pad on an integrated circuit device;

Figure 10 is a front view of a shoulder-point photolithographic spring probe;

Figure 11 is a partial cross-sectional side view of a shoulder-point photolithographic spring in contact with a trace on an integrated circuit device;

Figure 12 is a perspective view of a multiple shoulder-point photolithographic spring probe;

Figure 13 is a partial cross-sectional view of a multi-layered spring probe substrate providing controlled impedance and integrated components;

Figure 14 is a partial plan view of a substrate, in which a plurality of trace distribution regions are defined on the probe surface of the substrate, between a plurality of spring probes and a plurality of via contacts;

Figure 15 is a plan layout view of an integrated circuit having stress metal springs connected to IC pads, as laid out on the IC substrate surface, before release from the substrate surface;

Figure 16 is a plan layout view of an integrated circuit having stress metal springs connected to IC pads and extending from the substrate surface;

Figure 17 is a partial cutaway view of an integrated circuit having looped stress metal springs connected to IC pads and extending from the substrate surface, wherein a portion of the stress metal springs are embedded within a support substrate;

Figure 18 is a side view of integrated circuit devices on a semiconductor wafer;

Figure 19 is a side view of a semiconductor wafer having integrated circuit devices, which is mounted to a compliant wafer carrier substrate;

Figure 20 is a side view which shows the separation between integrated circuits for a semiconductor wafer which is mounted to a compliant wafer carrier substrate;

Figure 21 is a side view showing separated integrated circuits on a compliant wafer carrier substrate which is mounted to a test fixture;

Figure 22 is a side cross-sectional view of a stress metal spring interposer;

Figure 23 is a side cross-sectional view of a stress metal spring interposer having formed bumps on second surface contact region;

Figure 24 is a side cross-sectional view of a plated stress metal spring interposer;

Figure 25 is a side cross-sectional view of a stress metal spring interposer having filled bumps on a first surface contact region, and looped stress metal springs which partially extend beyond a polymer interposer layer;

Figure 26 is a side cross-sectional view of a stress metal spring interposer in which the interposer layer comprises a plurality of polymer layers;

Figure 27 is a side cross-sectional view of a stress metal spring interposer in which the stress metal springs have an effective spring angle less than 90 degrees;

Figure 28 is a partial view of a square leading end of a looped stress metal spring;

Figure 29 is a partial view of a pointed leading end of a looped stress metal spring;

Figure 30 is a partial view of a pointed leading end of a looped stress metal spring, which further comprises retaining grooves;

Figure 31 is a partial view of a pointed leading end of a looped stress metal spring, which further comprises retaining ledges;

Figure 32 is a plan view of a contact area of a looped stress metal spring, in which the contact area comprises an expanded rectangular contact region;

Figure 33 is a plan view of a contact area of a looped stress metal spring, in which the contact area comprises an expanded octagonal contact region;

Figure 34 is a plan view of a contact area of a looped stress metal spring, in which the contact area comprises an expanded diamond-shaped contact region;

Figure 35 is view of a first step of a stress metal spring interposer construction process, in which a sacrificial substrate is provided;

Figure 36 is a view of a second step of a stress metal spring interposer construction process, in which one or more stress metal spring layers are established on the sacrificial substrate;

Figure 37 is a view of a third step of a stress metal spring interposer construction process, in which non-planar portions of the stress metal springs extending from the sacrificial substrate are controllably formed;

Figure 38 is a view of a fourth step of a stress metal spring interposer construction process, in which an interposer substrate is applied on the sacrificial substrate and over the stress metal springs;

Figure 39 is a view of a fifth step of a stress metal spring interposer construction process, in which an outer portion of the applied interposer substrate is removed to access upper contact portions of the stress metal springs;

Figure 40 is a view of a sixth step of a stress metal spring interposer construction process, in which the sacrificial substrate is removed from the interposer substrate, exposing the lower contact portions of the stress metal springs;

Figure 41 is a side cross-sectional view of a stress metal spring contactor having contact areas extending from an elastomeric substrate;

Figure 42 is a side cross-sectional view of a stress metal spring contactor having bumped contact areas extending from an elastomeric substrate;

Figure 43 is a side cross-sectional view of a plated stress metal spring contactor having contact areas extending from an elastomeric substrate;

Figure 44 is a side cross-sectional view of a plated stress metal spring contactor having contact areas extending from the contactor substrate;

Figure 45 is a side cross-sectional view of a stress metal spring contactor having looped stress metal springs which partially extend beyond a polymer layer;

Figure 46 is a side cross-sectional view of a stress metal spring contactor in which the support layer comprises a plurality of polymer layers;

Figure 47 is a side cross-sectional view of a stress metal spring contactor in which the stress metal springs have an effective spring angle less than 90 degrees;

Figure 48 is a view of a first step of a stress metal spring contactor construction process, in which a contactor substrate having vias is provided;

Figure 49 is a view of a second step of a stress metal spring contactor construction process, in which in which one or more stress metal spring layers are established on the contactor substrate;

Figure 50 is a view of a third step of a stress metal spring contactor construction process, in which in which non-planar portions of the stress metal springs extending from the contactor substrate are controllably formed;

Figure 51 is a view of a preferred fourth step of a stress metal spring contactor construction process, in which the formed non-planar portions of the stress metal springs extending from the contactor substrate are controllably plated;

Figure 52 is a view of a fifth step of a stress metal spring contactor construction process, in which a secondary substrate is established over the formed non-planar portions of the stress metal springs extending from the contactor substrate;

Figure 53 is a view of a sixth step of a stress metal spring contactor construction process, in which an outer portion of the applied secondary substrate is removed to access upper contact portions of the stress metal springs;

Figure 54 is a side cross-sectional view of a stress metal spring contactor having a spring probe contact area extending from the contactor substrate, in which a connection is established between the stress metal spring contactor and a printed wiring board though a solder ball contact;

Figure 55 is a partial cutaway assembly view of a massively parallel test assembly having test electronics located in close proximity to the carrier-mounted integrated circuit devices under test;

Figure 56 is a partial perspective view of a massively parallel interconnection assembly;

Figure 57 is a partial expanded cross-sectional view of a massively parallel test assembly having an intermediate system board, which shows staged pitch and distribution across integrated circuit dies on a compliant carrier, a system board, and a flex circuit having a pad matrix;

Figure 58 is an expanded layer plan view of integrated circuit devices on a wafer, a circular substrate, and a system board;

Figure 59 is an expanded layer plan view of carrier-mounted integrated circuit devices which are directly connectable to a system board;

Figure 60 is a partial cross-sectional view of one embodiment of the flexible circuit structure;

Figure 61 is a partial cross-sectional view of an alternate embodiment of the flexible circuit, which comprises a flex circuit membrane structure;

Figure 62 is a partial perspective view of a flexible membrane circuit structure, wherein a flexible region is defined as an extension of the electronic test card structure;

Figure 63 is a partial perspective view of an alternate flexible circuit structure, wherein a flexible circuit is attached to an electronic test card structure;

Figure 64 is a partial cross-sectional view of one embodiment of a preferred flex circuit region of a test electronics module, in which the flex circuit is wrapped around the power and ground buss structure, and which preferably includes a thermal path across the flex circuit between a power module and a buss bar;

Figure 65 is a partial cross-sectional view of an alternate embodiment of the flex circuit region of a test electronics module, in which a plurality of power modules mounted on the inner surface of a flex circuit are positioned in thermal contact with a plurality of buss bars;

Figure 66 is a partial cross-sectional view of a second alternate embodiment of the flex circuit region of a test electronics module, in which a power module is electrically connected to the outer surface of a flex circuit, and is positioned in thermal contact with a buss bar;

Figure 67 is a perspective view of an alternate embodiment of a test electronics module, in which an integrated module base provides a pad matrix on a first planar region, and in which a power module is electrically connected to the pad matrix and to one or more buss bars, and is positioned in thermal contact with a buss bar;

Figure 68 is a partial cutaway assembly view of an alternate massively parallel test assembly having an intermediate system board, in which flexible spring probes are located on the lower surface of the system board;

Figure 69 is a partial cutaway assembly view of another alternate massively parallel test assembly having an intermediate system board, in which an interposer structure provides electrical connections between the substrate and the system board;

Figure 70 is a partial cutaway assembly view of a basic massively parallel test assembly, in which a substrate having spring probes is directly connected to the test electronics modules;

Figure 71 is a partial expanded cross-sectional view of a basic massively parallel test assembly, which shows staged pitch and distribution across a substrate and a flex circuit having a pad matrix;

Figure 72 is a partial cutaway assembly view of a massively parallel burn-in test assembly, in which burn-in test modules are connected directly to the system board, and in which separate temperature control systems are provided for the wafer-mounted integrated circuit devices under test and for the test electronics modules;

Figure 73 is a first partial expanded cross-sectional view showing massively parallel test assembly and alignment hardware and procedures;

Figure 74 is a second partial expanded cross-sectional view showing massively parallel test assembly and alignment hardware and procedures;

Figure 75 is a partial schematic block diagram of test circuitry for the massively parallel test system;

Figure 76 is a partial cutaway assembly view of a massively parallel interface assembly, in which a plurality of interface modules are connected, through a plurality of probe spring interposers and a system interconnect board structure;

Figure 77 is a partial cutaway assembly view of an alternate massively parallel interface assembly, in which a plurality of interface modules are connected through a system board and a system interconnect board structure;

Figure 78 is a schematic block diagram of connections between a plurality of computer systems, using a massively parallel interface assembly; and

Figure 79 is a schematic block diagram of connections between a plurality of electronic circuits, using a massively parallel interface assembly.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 1 is a plan view 10 of a linear array 12 of photolithographically patterned springs 14a-14n, prior to release from a substrate 16. The conductive springs 14a 14n are typically formed on the substrate layer 16, by successive layers of deposited metal 17, *e.g.* such as layers 17a,17b in FIG. 13, typically through low and high energy plasma and sputter deposition processes, followed by photolithographic patterning, as is widely known in the semiconductor industry. The successive layers 17 have different inherent levels of stress. The release regions 18 of the substrate 16 are then processed by undercut etching, whereby portions of the spring contacts 14a-14n, which are located over the release regions 18, are released from the substrate 16 and extend, *i.e.* bend, away from the substrate 16, as a result of the inherent stresses between the deposited metallic layers. Fixed regions 15 (FIG. 3, FIG. 4) of the deposited metal traces remain affixed to the substrate 16, and are typically used for routing (*i.e.* such as for redistribution or fan out) from the spring contacts 14a-14n. Figure 2 is a perspective view 22 of a linear array 12 of photolithographically patterned springs 14a-14n, after release from a substrate 16. The spring contacts 14a-14n may be formed in high density arrays, with a fine pitch 20, currently on the order of 0.001 inch.

Figure 3 is a side view 26a of a first photolithographically patterned spring 14 having a short length 28a, which is formed to define a first effective spring angle 30a (which can be from a few degrees to a full circle), spring radius 31a, and spring height 32a, after the

patterned spring 14 is released from the release region 18a of the substrate 16, away from the planar anchor region 15. Figure 4 is a side view 26b of a second photolithographically patterned spring 14, having a long spring length 28b, which is formed to define a second large effective spring angle 30b, spring radius 31b and spring height 32b, after the patterned spring 14 is released from the release region 18b of the substrate 16. The effective geometry of the formed spring tips 14 is highly customizable, based upon the intended application. As well, the spring tips are typically flexible, which allows them to be used for many applications.

Patterned spring probes 14 are capable of very small spring to spring pitch 20, which allows multiple spring probes 14 to be used to contact power or ground pads on an integrated circuit device 44 (FIG. 58, FIG. 59), thereby improving current carrying capability. As well, for a massively parallel interconnect assembly 278 (*e.g.* 278a, FIG. 55) having an array 12 (FIG. 1) of spring probes 14, multiple spring probes 14 may be used to probe I/O pads 47 on an IC substrate 48 (FIG. 9), such as on an integrated circuit device under test (DUT) 44 (FIG. 58, FIG. 59). Every spring probe contact 14 to be verified for continuity after engagement of the spring contacts 14 to the integrated circuit devices 44 under test (FIG. 55), thereby ensuring complete electrical contact between a massively parallel interface assembly 78 and a devices 44 on a compliant carrier 115 (FIG. 55), before testing procedures begin.

Improved Structures for Miniature Springs. Figure 5 is a first perspective view of opposing photolithographic springs 34a,34b, having an interleaved spring tip pattern, before spring to substrate detachment. Figure 6 is a perspective view of opposing interleaved photolithographic springs 34a, 34b, after spring to substrate detachment.

The interleaved photolithographic springs 34a, 34b each have a plurality of spring contact points 24. When spring contacts are used for connection to power or ground traces 46 or pads 47 of an integrated circuit device 44, the greatest electrical resistance occurs at the point of contact. Therefore, an interleaved spring contact 34, having a plurality of contact points 24, inherently lowers the resistance between the spring contact 34 and a trace 46 or pad 47. As described above, multiple interleaved spring probes 34 may be used for many applications, such as for high quality electrical connections for an integrated circuit device 44, or for a massively parallel interface assembly 78 (FIG. 15), such as for probing an integrated circuit device 44 during testing.

Figure 7 is a top view 42 of opposing interleaved photolithographic spring pairs 34a,34b in contact with the same traces 46 or pads 47 on an integrated circuit device under test (DUT) 44. The interleaved spring contact pair 34a and 34b allows both

springs 34a and 34b, each having a plurality of contact points 24, to contact the same trace 46 or pad 47. As shown in Figure 5, when a zig-zag gap 38 is formed between the two springs 34a,34b on a substrate 16, multiple tips 24 are established on each spring 34a,34b. Before the interleaved spring probes 34a,34b are released from the substrate 16, the interleaved points 24 are located within an overlapping interleave region 36. When the interleaved spring probes 34a,34b are released from the substrate 16, the interleaved spring points 24 remain in close proximity to each other, within a contact region 40, which is defined between the springs 34a, 34b. The interleaved spring contact pair 34a and 34b may then be positioned, such that both interleaved spring probes 34a and 34b contact the same trace 46, such as for a device under test 44, providing increased reliability. As well, since each interleaved spring 34a,34b includes multiple spring points 24, contact with a trace 46 is increased, while the potential for either overheating or current arcing across the multiple contact points 24 is minimized.

Figure 8 is a top view of parallel and opposing single-point photolithographic springs 14, before the springs 14 are released from a substrate 16. As described above for interleaved springs 34a, 34b, parallel springs 14 may also be placed such that the spring tips 24 of multiple springs contact a single trace 46 on a device 44. As well, opposing spring probes 14 may overlap each other on a substrate 16, such that upon release from the substrate 16 across a release region 18, the spring tips 24 are located in close proximity to each other. Figure 9 is a top view of parallel and opposing parallel single-point photolithographic springs 14, after the springs 14 are released from the substrate 16, wherein the parallel and opposing parallel single-point photolithographic springs 14 contact a single pad 47 on an integrated circuit device 44.

Figure 10 is a front view of a shoulder-point photolithographic spring 50, having a point 52 extending from a shoulder 54. Figure 11 is a partial cross-sectional side view of a shoulder-point photolithographic spring 50, in contact with a trace 46 on an integrated circuit device. Figure 12 is a perspective view of a multiple shoulder-point photolithographic spring 50. Single point spring probes 14 typically provide good physical contact with conductive traces 46 on an integrated circuit device 22, often by penetrating existing oxide layers on traces 46 or pads 47 by a single, sharp probe tip 24. However, for semiconductor wafers 104 or integrated circuit devices having thin or relatively soft traces 46 or pads 47, a single long probe tip 24 may penetrate beyond the depth of the trace 46, such as into the IC substrate 48, or into other circuitry.

Shoulder-point photolithographic springs 50 therefore include one or more extending points 52, as well as a shoulder 54, wherein the points 52 provide desired penetration

to provide good electrical contact to traces 46, while the shoulder 54 prevents the spring 50 from penetrating too deep into a device 44 or wafer 104. Since the geometry of the spring probes 50 are highly controllable by photolithographic screening and etching processes, the detailed geometry of the shoulder-point photolithographic spring 50 is readily achieved.

Figure 13 shows a partial cross-sectional view 56 of an ultra high frequency spring probe substrate 16. For embodiments wherein a spring probe 61 and related electrical conductors 60, 68, 64 on and through the substrate 16 are required to be impedance matched, one or more conductive reference surfaces 58a,58b,58c,58d and vias 65a,65b,65c may preferably be added, either within or on the substrate 16. The substrate 16 may also contain alternating ground reference traces 62a,62b, which are connected to reference planes 58a,58b,58c, to effectively provide a shielded coaxial transmission line environment 63. As well, the impedance control surfaces 58a,58b,58c,58d are not limited to the planar surfaces shown in Figure 13.

An insulating layer 66 may be deposited on a portion the probe spring 61, such as on the fixed region of the probe spring 61, up to but not enclosing the tip 24 (FIG. 2), as well as on the trace 60, which connects the spring probe 61 to the via 68. A conductive layer 58d may be deposited on top of the insulating layer 66, to provide a coaxial, controlled low impedance connection. Alternate layers of conductive materials 58 and dielectric materials 66 can preferably be integrated within the substrate 16, such as for embodiments which require decoupling capacitors in close proximity to a probe spring 61. For a substrate 16 which is a conductive material, such as silicon, a thin oxide layer 57 may preferably be deposited between the substrate 16 and a conductive reference plane 58c, thereby forming a high capacitance structure 59 between the spring probe 61 and the ground planes 58a and 58b. As well, one or more assembled components 69, such as passive components 69 (*e.g.* typically capacitors, resistors, and/or inductors), or active component devices 69, may be incorporated on either surface 62a,62 of the substrate.

The fixed portions 15 of the spring probes 61 typically extend a relatively short distance across the substrate 16. Traces 60 located on the surface of the substrate 16 are electrically connected to the fixed portions 15 of the spring probes 61, and electrically connect the probe springs 61 to the vias 68. The traces may be comprised of a different material than the spring probes 61, and are preferably comprised of metals having high electrical conductivity (*e.g.* such as copper or gold).

Figure 14 is a partial plan view 72 of a substrate 16, in which a plurality of distribution fanout traces 60 are defined on the probe surface 62a of the substrate 16, between a plurality of spring probes 61 and a plurality of via contacts 70. As described above, the spring probes 61, which are preferably photolithographically formed springs 61, may currently be formed with a pitch of approximately 0.001 inch. The traces 60 are preferably routed on the probe surface 62a, to connect to via contact areas 70, which are preferably laid out in a matrix across the surface of the substrate 16. In the substrate 16 shown in Figure 14, the via contact areas 70 are positioned with a probe surface first distribution pitch 74a, and a probe surface second distribution pitch 74b.

As the size and design of integrated circuit devices 44 becomes increasingly small and complex, the fine pitch 20 (FIG. 2) provided by miniature spring probe tips 61 becomes increasingly important. Furthermore, with the miniaturization of both integrated circuits 44 and the required test assemblies, differences in planarity between one or more integrated circuits 44 located on a wafer 104 and a substrate 16 containing a large number of spring probes 61 becomes critical.

As seen in Figure 14, lower standoffs 75 are preferably provided on the probe surface 62a of the substrate 16, such as to prevent the substrate 16 from damaging a wafer under test 104, or to set the spring probe tips 24 to operate at an optimal contact angle. The lower standoffs 75 are preferably made of a relatively soft material, such as polyamide, to avoid damage to the semiconductor wafer under test 104. In addition, to further avoid damage to active circuits 44 in the semiconductor wafer 104, the standoffs 75 are preferably placed, such that when the massively parallel interface assembly 78 is aligned with a device 44 on a semiconductor wafer 104, the standoffs 75 are aligned with the saw streets 136 (FIG. 18, FIG. 19) on the semiconductor wafer 104, where there are no active devices 44 or test structures. Furthermore, the height of the lower standoffs 75 are preferably chosen to limit the maximum compression of the spring probes 61a-61n, thus preventing damage to the spring probes 61a-61n.

The substrate 16 also typically includes one or more alignment marks 77 (FIG. 14), preferably on the probe surface 62a, such that the probe surface 62a of the substrate 16 may be precisely aligned with a wafer to be tested 104.

Chip Scale Semiconductor Package. Figure 15 is a plan layout view 78 of a chip scale integrated circuit package die region 80 having stress metal springs 84 connected to IC pads 82 and laid out on the upper substrate surface 85a, before release from the upper substrate surface 85a. In the plan layout view 78, the stress metal springs 84 each have a spring contact region 86, which before release are preferably laid out in an

IC surface first fanout pitch 87 and an IC surface second fanout pitch 88. Figure 16 is a plan layout view 90 of an integrated circuit die region 80 having stress metal springs 84 connected to IC pads 82 and extending from the substrate surface 85a, after release from the upper substrate surface 85a. During release from the upper substrate surface 85a, each of the stress metal springs 84 extend from respective release regions 18, whereby the contact regions 86 (FIG. 15) are rotated though an effective spring angle 30 (FIG. 3, FIG. 4), such that each stress metal spring 84 further preferably defines a spring contact surface 92. After release from the substrate surface 85a, each of the spring contact surfaces 92 are preferably laid out on a spring contact first fanout pitch 94 and on a spring contact second fanout pitch 96.

Figure 17 is a partial cutaway view of an chip scale integrated circuit package 100 having looped stress metal springs 84 connected to IC pads 82 and extending from the substrate spring surface 85a, wherein a portion of the stress metal springs 84 are embedded within a support substrate 106 comprised of an electrically insulative material. The support substrate 106 is typically comprised of a polymer substrate which provides support for each of the springs 84. In some preferred embodiments of the chip scale integrated circuit package 100, the support substrate 106 is a compliant polymer, *i.e.* an elastomer.

The support substrate 106 provides mechanical protection and adds mechanical support, *i.e.* strength, to the springs 84, provides passivation to the integrated circuit die regions 80, and adds mechanical strength to the assembly.

The combination of springs 84 and support substrate 106 constructed on the integrated circuit device, together form the integrated circuit package 100, which is attachable to a printed circuit board 216, typically using epoxy or solder. The support substrate 106 provides mechanical strength for chip attachment to the printed wiring board, and controls the amount of wetting for solder or epoxy on the springs 84. The compliant springs 84 provide the compliant connection to manage the thermal expansion mismatch between the die region 80 and a printed wiring board 216.

While the springs 84 shown in Figure 17 are preferably stress metal springs 84, the support substrate 106 can alternately be used to provide support for a wide variety of chip scale contacts 84. The support substrate 106 adds strength to the springs 84, and typically improves the robustness of the springs 84 to handling and use, that could otherwise result in breakage.

As seen in Figure 17, the springs 84 provide a conductive path between the integrated circuit 102 and the loop spring contact regions 92, which extend beyond the outer surface of the support substrate 106. As seen in Figure 15, Figure 16, Figure 32, Figure 33, and Figure 34, the loop spring contact regions 92 may preferably have an enhanced contact area geometry, such as to provide dimensional tolerance for electrical connections for testing, burn-in, or for subsequent device operation.

As seen in Figure 24, Figure 43, and Figure 51, stress metal springs 84,152 may preferably also comprise one or more plated metal coatings 166, such as a nickel, nickel alloy, silver, rhodium, palladium, cobalt, or gold alloy, which is applied to the metal springs 84,152 after release from the die region 80. The plated metallic coating 166 can also be used to increase the strength of the springs 84, such as to improve the robustness of the springs to handling and use. The plated metallic coating 166 can also be used to reduce the overall electrical resistance of the spring 84. In some embodiments, harder metals such as rhodium are used to provide resistance to mechanical wear and debris pickup from printed circuit board pads. As well, the use of a plated metallic coating 166 creates a higher contact force between the spring 84 and the pad on a circuit board, to reduce the electrical contact resistance. In some preferred embodiments of the stress metal springs 84,152, a first metal plating layer 166, such as a nickel alloy, is then followed by a secondary plating layer 166, such as gold or rhodium, such as to provide both increased spring strength as well as improved contact performance.

For stress springs 84,152 which preferably comprise a plated metal coating 166, a large portion of the required strength for the springs 84, 152 can be provided by the plating 166, such that the stress metal layers 17a-17n (FIG. 13) are not required to provide as much strength, such as compared to an unplated spring 84,152. Therefore, in some plated stress spring embodiments, the stress metal layers 17a-17n (FIG. 13) may only be used to define the structural shape before plating, thereby relaxing the process, *i.e.* metallurgical, parameters needed for the stress metal layers 17a-17n.

For embodiments of stress springs 84, 152 in which the plated metal coating 166 significantly strengthens the spring, support substrate 106 can alternately be comprised of a relatively hard polymer material 106, such as polyimide or a conventional molding material, such as to create a rigid IC package for direct surface mount applications to printed circuit boards 216. Chip-scale package integrated circuit devices 100 for use in harsh environments may also preferably further comprise plated metal spring coatings 166 combined with a polymer underfill 217 (FIG. 54).

As well, a boundary layer 161 (FIG. 26, FIG. 46) can preferably be used on the stress metal springs 84, 152, in which the boundary layer 161 is initially established as the first layer, *i.e.* the layer in contact with the release region 18. After release from the substrate surface 85a, the stress metal springs 84 loop through an effective angle 30, such that the boundary layer 161 becomes the outer layer of the contact region 92, for springs 84,152 having an effective angle greater than 180 degrees. The boundary layer 161 is preferably comprised of a highly conductive and non-corrosive metal, such as gold, rhodium, or palladium. In some embodiments, the boundary layer 161 is preferably be patterned on the substrate surface 85a, such as to be selectively applied to portions of the springs 84, *e.g.* such as to control the wetting of solder on a contact area 92 of a spring 84.

As seen in Figure 17, the stress metal springs 84 preferably have a effective angle 30 which is typically larger than 180 degrees, such that the leading edges 155 of the springs 84 preferably extend back into the support substrate 106, defining a loop spring contact region 92 along the convex arch of the spring 84. While the chip scale package semiconductor 100 shown in Figure 16 shows a large effective spring angle 30, a wide variety of chip scale package contact springs 84 can be enhanced by the use of support substrates 106 and one or more plating layers 166. Some springs 84,152 which require higher force or which need to contact smaller pads on a printed circuit board 216 preferably have an effective angle 30 which is typically less than 90 degrees.

Chip Scale Semiconductor Package Fabrication. The chip scale semiconductor package 100 can be efficiently fabricated using batch processing methods. A release layer 18, such as titanium or silicon oxinitride, is typically initially fabricated on the wafer die region 80. Next, one or more metal layers 17 with controlled stress, such as layers 17a,17b in Figure 13, are deposited on top of the release layer 18. In some embodiments of the chip scale semiconductor package 100, the stress metal layers 17 are comprised of the same or similar deposited metal, which have an initial stress gradient.

In some embodiments of the chip scale semiconductor package 100, the stress metal springs are built in compliance to photolithographic springs, such as described above, or as disclosed in U.S. Patent No. 5,848,685, U.S. Patent No. 5,613,861, or U.S. Patent No. 3,842,189, which are incorporated herein by reference.

The stress metal layers 17 are then typically patterned, to form spring and interconnect traces, using conventional photolithography and etch processes. A dielectric release window, such as polyimide, oxide, or nitride is defined, after the stress metal layers 17

are controllably etched. The release window defines the areas 18 where the spring metal is released from the substrate surface 58a, forming springs 84. After the stress metal springs 84 are controllably released from the substrate die region 80, the springs 84 are preferably plated 166, to adjust the spring constant, or to increase the strength of the stress metal springs 84. As described above, the exposed contact portions 92 of the stress metal springs 84 are preferably coated with gold or other material, such as for ease of soldering during a subsequent IC circuit assembly process. As well, a barrier metal 161 can also be formed on the stress metal spring 84, before stress metal deposition.

The support substrate layer 106 is then typically applied on the wafer 104, after the springs 84 are released and are preferably plated. The support substrate 106, typically comprising a polymer, functions as a protective layer for the integrated circuit device. In some embodiments of the chip scale semiconductor package 100, the support substrate 106 is controllably applied to a desired depth, such that the contact portions 92 of the stress metal springs 84 are exposed. In other embodiments of the chip scale semiconductor package 100, wherein the support substrate 106 is initially applied to cover the entire spring structures 84, the support substrate 106 is subsequently etched back, to expose the top contact region 92 of the springs 84. A photomask is preferably used for an etched support substrate 106, to controllably define the precise location and shape of the exposed region of the contact portions 92 of the stress metal springs 84.

Advantages of Chip Scale Semiconductor Package. The chip scale integrated circuit package 100 simplifies the process and reduces the number of processing steps in the fabrication of chip scale packages. A chip scale integrated circuit package 100 can be easily fabricated through batch processing techniques, similar to batch process manufacturing methods for semiconductor assemblies, such as integrated circuit devices.

The chip scale integrated circuit package 100 thus eliminates the serial process of bonding device leads to an integrated circuit one at a time. As well, the chip scale integrated circuit package 100 enables tight pitch packages with high electrical performance.

Furthermore, chip scale integrated circuit packages 100 can also provide a direct temporary contact to a board, such as to a printed circuit board 216, by pressure, which can eliminate the need for a socket or interposer connection. This temporary contact can also function as a probe contact, thus allowing the probe contact to be reduced to a simple pad array on a printed circuit board 216.

Compliant Wafer Chip Carrier. Figure 18 is a side view 110 of integrated circuit die regions 80 on a semiconductor wafer 104. Each of the integrated circuit die regions 80 have contacts 47, such as contact pads or stress metal springs 84. Saw streets 114 are defined between the integrated circuit die regions 80. In a preferred embodiment, the integrated circuit die regions 80 are chip scale semiconductor packages 100, having stress metal spring contacts 84 and a support substrate 106, as described above.

Figure 19 is a side view 112 of a semiconductor wafer 104, having integrated circuit die regions 80, in which the wafer 104 is adhesively mounted to a compliant wafer carrier substrate 115. The compliant substrate 115 has a first surface 116a and a second surface opposite the first surface 116b. The first surface 116a includes an adhesive layer, such that a wafer 104 may readily be mounted for subsequent IC separation and processing. A support 118 is also typically attached to the compliant substrate 115.

Figure 20 is a side view 120 which shows of the separation 122 of integrated circuits on a semiconductor wafer 104, which is mounted to a compliant carrier substrate 115. As known in the semiconductor processing industry, a saw is typically used to form separations 122 between integrated circuits 44 and die regions 80, along the saw streets 114.

The compliant wafer carrier 115 is typically comprised of a compliant polymer material, such as RISTON™, Part Number 1004R-9.0, from Nitto-Danko, Japan, or Ultron Systems, of Moore Park, CA. As described below, some preferred embodiments of the compliant wafer carrier 115 are thermally conductive and/or electrically conductive.

Figure 21 is a side view 130 which shows separated integrated circuits 44,100 on a compliant wafer carrier 115. The compliant wafer carrier 115 holds the integrated circuit dice 44,100 together in position after wafer separation 122, *e.g.* such as after saw and break, making it possible to handle all the separated dice 44,100 from a wafer 104 as a group, through back end assembly, test and burn in.

The use of a compliant wafer carrier 115 integrates assembly and wafer level testing and burn-in processes, and offers the speed advantage of parallel testing and simplicity in handling.

In conventional wafer level testing and burn in, the integrated circuit dice 44 are sometimes burned-in and tested before packaging and singulation from the wafer. However, a common difficulty encountered in a conventional wafer-level pre-singulation

approach is the complexity in managing the thermal expansion mismatch between the silicon wafer and the connector systems, which are required to make connections between the integrated circuit dies on the wafer and the system electronics. As well, defects induced by the packaging, singulation, and handling are not screened out by such a process.

The preferred use of a stress metal spring chip scale package 100, in conjunction with a compliant carrier 115, as described above, allows the use of low cost printed wiring board material 282, whose material coefficient of expansion can be different from the carrier mounted devices under test 100, to contact the dice during test and burn-in. As well, as described below, various embodiments of a massively parallel interface assembly 278, *e.g.* such as massively parallel interface assembly 278a shown in Figure 55, allow connection to a wide variety of carrier-mounted integrated circuits 44,100.

Therefore, the preferred use of chip scale package 100 and/or a massively parallel interface assembly 278 allow the test and burn of integrated circuit dice 44,100 after packaging and singulation 122, making it possible to detect assembly, saw and handling caused defects, while keeping the die in position for precision handling with massive parallelism.

In embodiments using a preferred chip scale package 100, the semiconductor wafer 104, having stress metal springs 84 which are processed onto the active surface 85a and are preferably partially encapsulated 106, is attached to a compliant decal wafer carrier 115. In some embodiments of the compliant carrier 115, the carrier 115 is similar to a conventional "blue" tape carrier which is commonly used for wafer sawing in the semiconductor processing industry.

The mounted wafer 104 is then sawed 122 into separate die 44,100, typically using a standard IC dicing and break process, without cutting through the carrier 115. The carrier tape 115 holds the packaged dice 100 in their relative position, as they were on the wafer 104. A contact fixture 132, such as the massively parallel test assembly 278 (FIG. 55, FIG. 57, FIG. 68, FIG. 70, FIG. 71), typically including a printed wiring board 282, comprises connections and associated electronics for connecting to and for testing the integrated circuits 44,100. The contact fixture 132 connections are designed to match the connections 47, such as spring leads 84, on the devices under test 44,100, when the contact fixture 132 is pressed onto the DUT devices 44,100 on the compliant carrier 115.

As seen in Figure 21, a pressure plate support 134, preferably constructed of a material

having a similar thermal coefficient of expansion (TCE) to the TCE of the printed wiring board 282, supports the back surface 116b of the compliant carrier 115. During testing and/or burn-in operations, the IC contact fixture 132 is fixedly attached 136 in relation to the pressure plate support 134, forming a sandwich structure 130, in which the mounted integrated circuit die 44,100 and the compliant carrier 115 are held in place. The pressure plate support 134 may also be preferably comprised of a compliant material, whereby the pressure plate support 134 and the carrier-mounted die 44,100 can readily conform to the system board 282.

When the temperature of this sandwich structure 130 is raised to the test and burn-in temperature, the printed wiring board 282, having a higher coefficient of expansion than the silicon die regions 80, expands faster than the silicon die regions 80. However, friction between the integrated circuit die 44,100 and the printed wiring board 282 and the pressure plate support 134 acts to drag the integrated circuit die 44,100, along with the printed wiring board 282, since the integrated circuit die 44,100 are separated 122 from each other, and are only connected through the compliant flexible carrier 115. Therefore, the relatively independent movement of each of the separated integrated circuit die 44,100 maintains pad to lead alignment between the integrated circuits 44,100 and the printed wiring board 282.

The separated integrated circuit die 44,100 which are mounted to the compliant carrier 115, are able to move relative to each other, while holding their positions on the compliant carrier 115. Therefore, the separated integrated circuit die 44,100 can be handled and processed as a "wafer" assembly, while maintaining sufficient connections to the IC contact fixture 132.

Therefore, the printed wiring board 282 and the pressure plate support 134 are not required to be comprised of a material having a similar coefficient of expansion TCE to the IC substrate 104. The compliant carrier-mounted dice 44,100 are able to move with the system board 282 and the support structure 134, such that the dice 44,100 remain in electrical contact with the system board 282 within the IC contact fixture 132. Furthermore, since the dice 44,100 are tested after packaging and singulation, the burn in and test applied to the dice will detect assembly induced defects in the dice 44,100.

As seen in Figure 21, a temperature controller 144 is preferably attached to the sandwich structure 130, such as to provide heating or cooling during testing and/or burn-in processes. In some embodiments of the compliant wafer carrier 115, the carrier 115 is comprised of a thermally conductive material, which functions as a thermal control plane during testing or burn-in, wherein the back side of the integrated circuits are in thermal

contact to temperature control 144, such as for cooling and/ or heating, through the compliant tape layer 115.

As well, the carrier 115 may preferably be comprised of electrically conductive material, whereby the carrier 115 may provide an electrical connection 140 to the back surface of the separated and mounted integrated circuit dice 80.

Stress Metal Spring Interposer. Figure 22 is a partial cross-sectional view 150 of a stress metal spring interposer 151a, comprising one or more springs 152 which extend from a first surface 156a to a second surface of an interposer substrate 154. The springs 152 also typically comprise contact pads 158 which extend from the first surface of the interposer substrate 154. Stress metal spring interposers 151 provide ultra-high density, compliant through connections, and provide high density connections over extreme temperature ranges.

Conventional interposers, such as pogo pins, springs, or wires which are fabricated by mechanical construction methods are limited in pitch, which limits the connection density and requires high connection force.

Stress metal spring interposers 151 use thin film stress metal to form a tight array of thin film springs, held together by a substrate 154 comprises of a polymer material. Electrical connections are made from one side 156a of the polymer sheet to the other side 156b by the conductive springs 152.

A high density connection between the two surfaces 156a,156b can therefore be made by having each of the surfaces pressing against one side of the polymer sheet with stress springs embedded. Different tip shapes can be engineered on each end of the spring 152, such as for different contact materials.

In some embodiments of the stress metal spring interposers 151, the stress metal springs are built in accordance to U.S. Patent No. 3,842,189 and/or U.S. Patent No. 3,842,189, which are incorporated herein by reference.

A wide variety of geometries and materials may be used for the construction of the spring interposer 152. For example, Figure 23 is a side cross-sectional view 160 of a stress metal spring interposer 151b having formed bumps 162 on the second surface contact region 158. Figure 24 is a side cross-sectional view 64 of a plated stress metal spring interposer 151c. The springs 152, as well as stress springs 84, are preferably

comprised of layers of metal having 17 (FIG. 13) having different initial levels of stress, such that the springs form an effective spring angle 30 (FIG. 3) during fabrication.

Figure 25 is a side cross-sectional view of a stress metal spring interposer 151d having filled bumps 159 on a first surface contact region, and looped stress metal springs 152 which partially extend beyond a polymer interposer layer 154, defining a hollow contact region 157 between the contact area 92 of the looped stress metal springs and the top surface 156b of the polymer layer 154.

Figure 26 is a side cross-sectional view of a stress metal spring interposer 151e, in which the interposer layer comprises a plurality of polymer layers 154a,154b. As well, the looped stress metal springs further comprise a boundary layer 161. In some embodiments of the stress metal springs 84,152, the boundary layer 161 comprises a metal having high electrical conductivity and/or corrosion resistance. The boundary layer 161 may also be used for increased stress spring strength.

Figure 27 is a side cross-sectional view of a stress metal spring interposer 151f, in which the stress metal springs 152 have an effective spring angle less than 90 degrees, and in which the interposer substrate 154 adds strength and/or protection for the stress metal springs 152.

Leading Edge and Contact Geometries for Loop Stress Metal Springs. Loop stress metal prings152, such as used for the stress metal chip scale package 100, the stress metal interposer 151, or for the stress metal contactor 196, such as contactor 196a in Figure 41, can have a wide variety of leading edge and contact area geometries.

Looped Stress Metal Spring Leading End Detail. Figure 28 is a partial view of a square leading end 155a of a looped stress metal spring 84,152. Figure 29 is a partial view of a pointed leading end 155b of a looped stress metal spring 84,152. Figure 30 is a partial view of a pointed leading end 155c of a looped stress metal spring 84,152, which further comprises retaining grooves 157. Figure 31 is a partial view of a pointed leading end 155d of a looped stress metal spring 84,152, which further comprises retaining ledges 163.

The leading end 155 of high effective angle looped stress metal springs 84,152 can have a variety of leading end geometries 155, since the leading ends 155 are typically not used for contacting. The desired geometry of the leading end 155 is typically chosen to control the formation of the non-planar springs 152, during lift-off from a substrate, *i.e.* the spring tip geometry helps the stress metal spring 152 to lift in the

correct direction. In some embodiments, the geometry of the leading end 155 is chosen to anchor the loop spring probe within a supporting substrate 154, such as with grooves 157 or ledges 163.

Contact Area Structures. Figure 32 is a plan view of a contact area of a looped stress metal spring 152, in which the contact area 92 which extends beyond the outer surface 156b of the polymer layer 106,154 comprises an expanded rectangular contact region 92a. Figure 33 is a plan view of a contact area 92b of a looped stress metal spring 152, in which the contact area 92b which extends beyond the outer surface 156b of the polymer layer 106,154 comprises an expanded octagonal contact region 92b. Figure 34 is a plan view of a contact area 96c of a looped stress metal spring, in which the contact area 92c comprises an expanded diamond-shaped contact region 92c. As the stress metal springs 84,152 are typically comprised of photolithographically formed layers 17, *e.g.* such as 17a,17b in Figure 13, the defined contact area 92 can have a variety of geometries, such as to provide dimensional tolerance for the interconnection structure.

Stress Metal Spring Interposer Construction Process. Figure 35 is view of a first step 170 of a stress metal spring interposer construction process, in which a sacrificial substrate 172 is provided. For embodiments of the stress metal spring interposer 151 in which the springs 152 include contact pads 158, 159, the sacrificial substrate 172 includes a pad formation structure 174. The sacrificial substrate 172 can be fabricated from a wide variety of etchable materials, such aluminum or silicon. As described below, the sacrificial substrate 172 is used as a temporary substrate in the fabrication of a spring interposer 151, and is eventually removed, typically by an etching process.

Figure 36 is a view of a second step 176 of a stress metal spring interposer construction process, in which one or more stress metal spring layers 178, such as stress metal layers 17, are established on the sacrificial substrate 172, and in which spring release regions 18 are controllably defined. For some embodiments of the stress metal spring interposer 151 in which the springs 152 include contact pads 158, the successive layers 17 of the spring 152 are formed directly into pad formation structures 174. In alternate embodiments of the stress metal spring interposer 151 in which the springs 152 include contact pads 158, discrete contact pads 159 (FIG. 26, FIG. 27) are formed within pad formation structures 174, such as by a fill and polish process, in which the successive layers 17 of the spring 152 are formed over the discrete contact pads 158.

Figure 37 is a view of a third step 180 of a stress metal spring interposer construction process, in which non-planar portions of the stress metal springs 152 extending from the

sacrificial substrate 172 are controllably formed, upon release from the release regions 18. The inherent stress of the metal layers 17 forms a spring having an effective spring angle 30. In the embodiment shown in Figure 37, the effective spring angle is greater than 180 degrees, *e.g.* such as 270 degrees, such that the spring 152 has a convex contact surface 92 (FIG. 39).

Various spring shapes and lift can be used, including springs 152 with sharp contact tips 24, which point towards the contact pad surface at various angles 30. The springs 152 provide ultra high-density connectivity between the two different surfaces, while maintaining compliance. Different contact shapes can be fabricated on the contact surfaces, by first defining the desired contact shapes on the substrate material 172.

The stress metal springs 152 shown in Figure 37 also preferably comprise a plating layer 166 (FIG. 24), which is typically applied to the formed non-planar springs 152, before the formation of the support substrate 154, such as an elastomer 154, such that the plating 166 is applied to the non-planar portions of the stress metal springs 152. Plating 166 can be used for spring strengthening, enhanced conductivity, and/or for corrosion protection.

Figure 38 is a view of a fourth step 182 of a stress metal spring interposer construction process, in which an interposer substrate 184 is applied on the sacrificial substrate 172 and typically over the stress metal springs 152.

Figure 39 is a view of a fifth step 186 of a stress metal spring interposer construction process, in which an outer portion of the applied interposer substrate 184 is removed 188 to form a contoured interposer substrate 154, such as by etching, to access upper contact portions 92 of the stress metal springs 152.

Figure 40 is a view of a sixth step 190 of a stress metal spring interposer construction process, in which the sacrificial substrate 172 is removed 192, such as by etching from the interposer substrate 154, exposing the lower contact portions 158 of the stress metal springs 152.

The spring interposer 151 can be configured for a wide variety of applications, and can be used to provide a high density interface, *e.g.* such as 50-100 microns. The spring interposer 151 can be fabricated to have a variety of contact area geometries 92 as well, such as a square, rectangle, or circular configurations, based on the desired application.

As well, some embodiments of the spring interposer 151 have an effective spring angle 30 less than 180 degrees, whereby the springs include a contact tip 24 to establish electrical connections. As well, some embodiments of the spring interposer 151 preferably have a planar lower contact region 158. As described above, a boundary layer 161, such as a metal having enhanced conductivity, corrosion resistance, or solderability characteristics (*e.g.* such as gold, rhodium, or palladium), may also preferably be established as the lowest layer of stress metal layers, such that the boundary layer 161 provides the contact surface 92.

In altemate embodiments of the spring interposer 151, the interposer substrate 154, 184 comprises a plurality of interposer layers 154a,154b (FIG. 26). A first thin layer 154a, comprising a relatively rigid electrically insulative material, such as polyimide, provides increased dimensional control, handleability, and mountability for the interposer 151, while the second interposer layer 154b, typically comprising a relatively non-rigid electrically insulative elastomer, provides enhanced support and compliance for the springs 152. In embodiments of the spring interposer 151 having a composite interposer structure 154, the thin semi-rigid layer 154a may also preferably comprise one or more openings.

Stress Metal Spring Contactor. Figure 41 is a side cross-sectional view 194 of a stress metal spring contactor 196a having contact areas 92 extending from an elastomeric support substrate 154, which are electrically connected to vias 200 that extend through a wafer substrate 198. Figure 42 is a side cross-sectional view of a stress metal spring contactor 196b having bumped contact areas 162 extending from a support substrate 154. Figure 43 is a side cross-sectional view of a plated stress metal spring contactor 196c having plated contact areas 92 extending from a support substrate 154. Figure 44 is a side cross-sectional view of a plated stress metal spring contactor 196d having contact areas 92 extending from the contactor substrate 198.

Figure 45 is a side cross-sectional view of a stress metal spring contactor 196e having looped stress metal springs 152 which partially extend beyond a polymer layer, defining hollow regions 157 between the contact area 92 of the stress metal springs 152 and the upper surface 156b of the support substrate 154. Figure 46 is a side cross-sectional view of a stress metal spring contactor 196f in which the support layer comprises a plurality of polymer layers 154a,154b. Figure 47 is a side cross-sectional view of a stress metal spring contactor 196g in which the stress metal springs 152 further comprise a boundary layer 161, such as gold, rhodium, or palladium, and have an effective spring angle 30 less than 90 degrees.

As seen in Figure 54, the stress metal spring contactor 196 spring structure can be used for probing solder balls 220 on a bumped wafer, such as to provide a temporary contact to solder bumps on flip chip devices.

Traditional vertical probes, such as the Cobra Probe™ from IBM and the Microspring™ from Form Factor are expensive, and have a long lead time. The stress metal spring contactor 196 can be fabricated using batch processing methods, which decreases the cost of the contactor, and provides a short turnaround time.

Stress Metal Spring Contactor Construction Process. Figure 48 is a view of a first step 202 of a stress metal spring contactor construction process, in which a spring probe contactor substrate 198 having vias 200 is provided.

Figure 49 is a view of a second step 204 of a stress metal spring contactor construction process, in which in which one or more stress metal springs 178 are established on the spring probe contactor substrate 198, wherein each of the springs 178 comprise a plurality of layers 17 having different levels of inherent stress. Figure 50 is a view of a third step 206 of a stress metal spring contactor construction process, in which in which non-planar portions 152 of the stress metal layers extending from the contactor substrate are controllably formed.

Figure 51 is a view of a fourth step 208 of a stress metal spring contactor construction process, in which the formed non-planar portions of the probe springs 152 extending from the contactor substrate are preferably plated 166. The plating layer 166 is typically applied to the formed springs 152, before the formation of an elastomer support layer 154,184, such that the plating 166 is applied to the non-planar portions of the stress metal 152. Plating 166 is preferably used for contactor embodiments which require spring strengthening, enhanced conductivity, and/or corrosion protection.

Figure 52 is a view of a fifth step 210 of a stress metal spring contactor construction process, in which a secondary substrate 184 is established over the formed non-planar portions of the probe springs 152 extending from the contactor 198. Figure 53 is a view of a sixth step 212 of a stress metal spring contactor construction process, in which an outer portion of the applied secondary substrate 184 is removed 214 to established a contoured substrate 154, to access upper contact portions 92 of the stress metal springs 152.

Figure 54 is a side cross-sectional view 214 of a probe spring contactor 196 having a spring probe contact area 92 extending from the support substrate 154, in which a

connection is established between the compliant stress metal spring contactor lead 152 and a printed wiring board (PWB) 216, though a solder ball contact 220 and a board contact 218.

Massively Parallel Interface Assemblies for Testing and Burn-In of Compliant Wafer Carrier. Figure 55 is a partial expanded cross-sectional view of a massively parallel test assembly 278a having an intermediate system board 282 for connection to separated integrated circuit devices 44,100 on a compliant carrier 115. Figure 56 is a partial perspective view 310 of a massively parallel interface assembly 278a. Figure 57 is a partial expanded cross-sectional view 320 of a massively parallel test assembly 278a having an intermediate system board 282, which shows staged pitch and distribution across a system board 282, and a flex circuit 290 having a pad matrix 288 (FIG. 55) of electrical connectors 319a-319n. As shown in Figure 55 and Figure 57, the interface assembly 278a is positioned in relation to a compliant wafer carrier 115, having one or more integrated circuits 44, which are separated by IC separation 122 (FIG. 20, FIG. 21). The test structures shown in Figure 21 and Figure 55 allow parallel testing and burn-in for separated integrated circuit devices 44,100 which are mounted on a compliant carrier 115. The chip scale packaged devices 44,100 are loosely held together by the compliant carrier 115, and make contact to the system transformer board 282. These devices can be connected as shown to a standard tester, or through a set of electronics, to minimize the number of connections between the separated integrated circuit devices 44,100 and the tester.

The massively parallel interface assembly 278a provides electrical interconnections to each of the integrated circuit devices 44,100 located on the compliant carrier 115, to work effectively in a typical integrated circuit testing environment. The interface assembly 278a is readily used for applications requiring very high pin counts, for tight pitches, or for high frequencies. As well, the interface assembly 278a is easily adapted to provide electrical contact for all traces 46 (FIG. 7) and input and output pads 47 (FIG. 7, FIG. 9) for one or more integrated circuit devices under test 44 on the compliant carrier 115.

The conductive pads 284a-284n on the lower surface of the system board 282 are typically arranged with a pad pitch 324 (FIG. 57), such that the conductive pads 284a 284n are aligned with the electrical contacts 47, such as the contact regions 92 of stress metal springs 84, on the carrier-mounted integrated circuit devices 44,100.

The conductive pads 284a-284n on the lower surface of the system board 282 are then routed to conductive paths 286a-286n, which are typically arranged with a system board pitch 326. The electrically conductive connections 328a-328n, which may be arranged

within one or more connection regions 332, are located on the upper surface of the system board 282, and are routed to the conductive paths 286a-286n. The electrically conductive connections 328a-328n are typically arranged within the connection region 332, with a system board pad matrix pitch 320, which is typically aligned with the flex circuit pad matrix pitch 334 for each of the test electronics modules 292a-292k (FIG. 55).

The system board matrix pitch 320 is typically chosen such that the electrically conductive connections 328a-328n are aligned with the flex circuit electrical connectors 319a-319n located on the flex circuits 290, which are typically arranged in a plurality of pad matrices 288 (FIG. 56), having a flex circuit pad matrix pitch 334.

The test electronics modules 292a-292k are a basic building block for most of the embodiments of the massively parallel interface test assemblies 278a-278d. The test electronics modules 292a-292k are mounted in parallel (*e.g.* as seen in Figure 55), to form an array of modules 292a-292k, which each provide electronics support to one or more columns 339 (FIG. 58, FIG. 59) of integrated circuit devices 44,100 on a compliant carrier 115 or in a wafer form 104, or to a portion of a column 339 or die 44, along which the test electronics modules 292a-292k are mounted.

Figure 56 is a partial perspective view 310 of a massively parallel interface assembly 278a, wherein test electronics modules 292 are mounted on a frame 302. Each of the test electronics modules 292 shown includes a preferred flex circuit 290, having a pad matrix 288 of electrical contactors 319, and one or more power control modules 300. The flex circuit 290 for each of the test electronics modules 292 is mounted on one or more buss bars 298a-298h, and extends downwardly through the frame 302. The buss bars 298a-298h are attached to the frame 302, such as by electrically isolated fasteners 312, thereby providing a substantially rigid structure. The frame 302 preferably includes test module alignment guides 318, as well as frame to system alignment pins 314 and means 316 for fastening the frame 302 to a wafer chuck 306 (FIG. 55) or to a pressure plate support 134 (FIG. 21). The assembly 310 may also preferably include other means for holding the test electronics modules 292a-292k, such as a card cage (not shown) located below the frame 302.

The separated carrier-mounted integrated circuit devices 44,100 interface to a system board 282, which provides a standard interface to the tester electronics, at a coarser pitch than the contact pitch of the integrated circuit devices 44,100. The system board 282 can be comprised a wide variety of materials, such as ceramic, high density printed wiring board, silicon, glass, or glass epoxy. Each of the tester electronics modules 292a-292n are attached to the system board 282, via a membrane or flex circuit 290.

Contacts 319,328 between test electronics modules 292a-292k and the system board 282 are achieved using solder, pressure contact, or spring probes. For embodiments which use spring probes 319,328, the spring probes may have a variety of tip geometries, such as single point springs 14, interleaved springs 34, or shoulder point springs 50, and are typically fabricated using thin-film or MEMS processing methods, to achieve low manufacturing cost, well controlled uniformity, very fine pad pitches 20, and large pin counts. In some embodiments, the connections 319,328 are built in compliance to photolithographic springs, such as described above, or as disclosed in either U.S. Patent No. 5,848,685 or U.S. Patent No. 5,613,861, which are incorporated herein by reference.

The configuration shown in Figure 55 brings power through the switchable power modules 300, and input/output signal traces 348 (FIG. 62, FIG. 63) from the pin electronics card 294 to the system board 282. This configuration has the advantage of reducing routing congestion in the flex circuit or membrane 290.

The structure of the interface assembly 278a provides very short electrical distances between the carrier-mounted integrated circuit devices 44,100 and the controlled impedance environment in the system board 282, which allows the interface assembly 278a to be used for high frequency applications.

Figure 58 is an expanded layer plan view of a integrated circuit dies 44 on a wafer 104, a circular substrate 16, and a rectangular system board 282, wherein the intermediate substrate 16 is typically used in test system embodiments wherein an interface assembly 278 is required to be connected to an entire wafer 104, *i.e.* for integrated circuits which are not separated and mounted to a compliant carrier 115. For substrates 16 which are preferably comprised of silicon (which may be preferably chosen to match the thermal coefficient of expansion (TCE) of a integrated circuit dies 44 under test), the silicon substrate 16 may preferably be fabricated by a similar process to that of a wafer 104, such that the substrate 16 may be fabricated from a circular wafer substrate 16.

As seen in Figure 58, devices 44, each having a plurality of pads 47, are formed on a wafer 104, and are typically populated across the wafer 104 by a series of rows 337 and columns 339, wherein saw streets 114 are located between the rows 337 and columns 339. For substrates 16 which are preferably comprised of ceramic materials, the silicon substrate 16 may preferably be fabricated from one or more rectangular ceramic substrates 16. The substrate 16 may include a travel limit mechanism, such as

one or more upper standoffs located on the connector surface of the substrate 16, such as to limit perpendicular travel of the substrate in relation to the system board 282.

Figure 59 is an expanded layer plan view of separated integrated circuit dies 44,100 on a compliant carrier 115, which can be directly connected to a system board 282. As described above, the carrier-mounted separated integrated circuit dies 44,100 are typically mounted between the system board 282 and a pressure plate support 134 (FIG. 21).

As can be seen in the system board 282 in Figure 58 and Figure 59, the electrically conductive connections 328a-328n, which are located on the upper surface of the system board 282, are typically arranged within one or more connection regions 332, to connect to flex circuit contactors 319 (FIG. 57), which are preferably arranged within a similar number of one or more pad matrices 288 (FIG. 56).

In some preferred embodiments of the massively parallel interface assembly 278, each of the test electronics modules 292 (*e.g.* 292a) is identical to the other test electronics modules (*e.g.* 292b-292k), thereby having an identical number of test componentry (thereby having an identical test capacity). In some embodiments of the massively parallel interface assembly 278, a similar number of devices 44 is routed to each test electronics modules 292a-292k.

In alternate embodiments of the massively parallel interface assembly 278, a different number of devices 44 may routed to a test electronics module 292 (*e.g.* 292a), such as for outer columns 339 of devices under test 44 on a wafer carrier 115. For a plurality of standardized test electronics modules 292a-292k having an identical number of test componentry, a test electronics module 292 which has a greater capacity than the number of devices 44 which are connected may still be used, typically through programming the test electronics module 292 to bypass testing for unused test circuitry 294, or through system control 430 (FIG. 75).

Figure 60 is a partial cross-sectional view of one embodiment of the flexible circuit structure 342a, having a polyamide layer 344a, and opposing conductive layers 346a and 346b. Figure 61 is a partial cross-sectional view of an alternate embodiment of the flexible circuit 290, which comprises a dielectric flex circuit membrane structure 342b, and opposing conductive layers 346a and 346b. In some embodiments of the flex circuit 290, the flex circuit membrane structure 342 is inherently flexible. In alternate embodiments of the flex circuit 290, the flex circuit structure 342 is rigid in regions where one or both conductive layers are substantially located. The controlled removal of the

conductive layers 346a,346b produces controlled flexibility for the flex circuit 290, while providing regions of formed conductive paths.

Figure 62 is a partial perspective view of a flexible membrane circuit structure, wherein a flexible region 290a is defined on the test card structure 294a. Figure 63 is a partial perspective view of an alternate flexible circuit structure, wherein a flexible circuit 390b is attached to a test card structure 294b by attachments 350 (*e.g.* such as but not limited to fasteners, heat staking, microwelding, or adhesives).

The test electronics 294a,294b populated on each of the test electronics modules 292a-292k provide stimulus and response detection for one or more devices under test 44. The test electronics 294a,294b are built on a high density interconnect (HDI) substrate 342a,342b, or on a standard printed wiring board 294a, which is connected to the flexible circuit 290. The test electronic card 294a,94b is populated with control and response electronics (*e.g.* such as test electronics 440 in FIG. 75). Each test electronics module 292 (*e.g.* 292a) is connected to the backend electronics and computer interface links 296 (*e.g.* typically by parallel or serial links). Alternatively, the signal pins in the tester electronics modules 292a-292k can be connected serially, on a daisy chain, to simplify the electrical connections, such as to external test hardware. Test vector and setup information is sent to the pin electronics, from a system computer and control electronics (*e.g.* such as external pattern generator 446 in FIG. 75), through the links 296.

Within each of the test electronics modules 292a-292k, a test electronics card 294 is connected to the flex circuit/membrane 290. Test electronics cards 294 may preferably be fabricated as an integral structure with the flexible circuit 290, such as on an etched thin film substrate, whereby portions of the substrate are etched, to create the flexible membrane circuit 290. In an alternate embodiment of the test electronics module, a separate test electronics card substrate 294 is connected to a flex circuit, typically by solder, wire bond or connectors.

Figure 64 is a partial cross-sectional view of one embodiment of the flex circuit region 290 of a test electronic module 292, which preferably includes a thermally conductive pathway 354 across a flex circuit 290 between a power control module 300 and one or more buss bars 298. Each of the buss bars 298a-298h, which are typically separately electrically connected to a plurality of external power supplies 434a-434h (FIG. 75), are typically electrically isolated from each other by insulators 352. The insulators 352 may be a separate layer from the buss bars 298a-298h, or may alternately be an electrically insulative layer 352 on the buss bars 298a-298h.

Figure 65 is a partial cross-sectional view of an alternate embodiment of the flex circuit region 290 of a test electronic module 292, in which one or more power control modules 300a-300h are mounted on the inner surface of the flex circuit 290, and are positioned in thermal contact with a plurality of buss bars 298a-298h.

Figure 66 is a partial cross-sectional view of a second alternate embodiment of the flex circuit region 290 of a test electronic module 292, in which a power control module 300 is electrically connected to the outer surface of a flex circuit 300. A power control access region 356 is preferably defined through the flex circuit region 290, whereby the power control module 300 positioned in intimate thermal contact with a buss bar 298 (*e.g.* such as buss bar 298b).

One or more power and ground bus bars 298a-298h are used to distribute power to all the devices under test 44. Power control modules 300, typically comprising decoupling capacitors, switching control circuits and regulators for each device under test 44, are preferably mounted on the flex circuit 290, as shown in Figure 64, Figure 65, or Figure 66.

While some preferred embodiments of the test electronics modules 292a-292k include flex circuit structures 290, the unique interface structure provided by the flex circuit structure 290 may alternately be achieved by other suitable interface designs. Figure 67 is a perspective view of one alternate embodiment of a test electronics module 292, in which an integrated module base 357 provides a pad matrix 288 of electrical contacts 319 on a pad matrix planar region 358. One or more power control modules 300 are electrically connected to electrical contacts 319 located on the pad matrix 288, through power control module (PCM) traces 349, and to one or more buss bars 298a-298h. The power control modules 300 are also preferably positioned in thermal contact with one or more buss bars 298a-298h. Signal traces 348 (FIG. 62, FIG. 63) are also connected to electrical contacts 319 located the pad matrix 288. The signal traces 348 extend across a link and component planar region 359, and are either connected to test electronics 294, or extend to link 296.

In the various embodiments of the test electronics modules 292, one or more bus bars 298 provide the power and heat sink paths for the power control modules 300. Power for devices under test 44 is typically provided through separate rail buss bars 298, or may alternately share the same rail buss bars 298 with the power control modules 300. The power rail buss bars 298 also preferably provide mechanical support for the flex circuit 290 and the system board 282 and/ or the test electronics cards 294a-294k. In

some embodiments of the test electronics modules 292a-292k, the power control module circuits 300 are connected in the serial scan path, to provide individual power and ground control to the devices under test 44.

Alternate Massively Parallel Test Assemblies. Figure 68 is a partial cutaway assembly view of an alternate massively parallel test assembly 278b having an intermediate system board 282, in which flexible spring probes 360 are located on the lower surface 339a (FIG. 57) of the system board 282. The structure and features of the massively parallel test assembly 278b are otherwise identical to the massively parallel test assembly 278a shown in Figure 55. The system board spring probes 360 can be used to provide planarity compliance between the system board 282 and the carrier-mounted integrated circuit devices 44,100, and provide high quality electrical connections, over a wide range of temperatures.

Figure 69 is a partial cross-sectional view of an alternate interface assembly 278c, wherein a large grid array (LGA) interposer connector 362 is located between a substrate 16 and the system board 282. The LGA interposer connector 362 provides a plurality of conductors 164a-164n between the electrical connections 64a-64n on the substrate 16 and plurality of conductive pads 284a-284n on the lower surface of the system board 282. In one embodiment, the LGA interposer connector 362 is an AMPIFLEX™ connector, manufactured by AMP, Inc., of Harrisburg PA. In another embodiment, the interposer connector 362 is a GOREMATE™ connector, manufactured by W.L. Gore and Associates, Inc., of Eau Clare, WI. In another alternate embodiment, a pogo pin interposer 362 is used to connect opposing conductive pads 284a-284n on the system board 282 to electrical connections 64a-64n on the substrate 16.

Figure 70 is a partial cutaway assembly view of a basic massively parallel test assembly 278d, in which a substrate 16 has spring probes 61a-61n on a lower probe surface 62a, and vias 68a-68n which are connected between the spring probes 61a-61n and conductors 64a-64n located on an upper surface 62b of the substrate 16, wherein the substrate 16 is directly connected to the test electronics modules 292a-292k. Figure 71 is a partial expanded cross-sectional view 366 of the basic massively parallel test assembly 278d, which shows staged pitch and distribution across a substrate 16 and a test electronics module 292 having a pad matrix 288 of electrical contactors 319.

Figure 72 is a partial cross sectional view 370 of an alternate massively parallel interface assembly 378e, which shows one embodiment of a basic clamping structure 372. The

interface assembly 378e is typically intended for burn-in testing only, whereby test electronics 294 are packaged in small modules 374. The modules 374 are mounted directly onto the system board 282, and are preferably used for burn-in testing, which typically requires significantly less test electronics than the test electronics modules 292a-292k (*e.g.* such as shown in FIG. 55). The clamping structure 372 shown in Figure 72 may also be used for the wafer level massively parallel interface assemblies 278.

For the massively parallel interface assembly 378e shown in Figure 71, the interposer substrate 16 is preferably fabricated from a thin substrate 16, such as a 10 mil thick glass plate, whereby the substrate 16 may flex slightly, to conform to the surface of integrated circuit dies 44 on a wafer 104, to accommodate for non-planarity or bowing between the wafer and the interposer substrate 16.

A seal 380 around the periphery of the interposer substrate 16 preferably provides an air-tight chamber 382. Air pressure is preferably applied between the system board 282 and the interposer substrate 16. An applied pressure 384 also thermally isolates the integrated circuit dies 44 on a wafer 104 from the test electronics 374,294. While integrated circuit dies 44 are typically required to operate at elevated temperatures during burn-in testing (*e.g.* such as at 125-160 degrees Celsius), the test electronics 294 should preferably operate at a lower temperature (*e.g.* such as below 75 degrees Celsius).

The wafer chuck 306, such as wafer chuck 306b in Figure 72, preferably includes a wafer thermal control system 392, which preferably comprises a wafer heating system 394 and/or a wafer cooling system 396, such as to provide temperature control to the wafer under test 104. The wafer thermal control system 392 is preferably controlled by a test system temperature controller 388, which is typically linked 389 to the system controller 432 (FIG. 75).

The test electronics 374,294 are preferably located in one or more cooling chambers 376. A cooling system 390 is preferably used to control the operating temperature of the test electronics 374,294 within the cooling chambers 376, and is also preferably controlled by the test system temperature controller 388.

A wafer loading vacuum circuit 386, having vacuum tracks 408 (FIG. 73), is preferably built into the wafer chuck 306, to provide vacuum suction to hold the wafer 104 in position, and to improve planarity between the substrate connector 16 and the wafer 104.

Test System Architecture. The test system consists of an alignment set up, which performs wafer alignment, cooling unit, and tester electronics. The alignment subsystem and cooling units can be built with technology known in the art.

System Alignment. Figure 73 is a first partial expanded cross-sectional view showing massively parallel test assembly 400 and alignment hardware and procedures for wafers 104. The test assembly 400 includes a carrier ring 402, which preferably includes one or more alignment features, such as alignment pins 406, whereby the carrier ring 402 may be aligned to a system board 282. The system board 282 preferably has mating alignment features, such as alignment holes 426 (FIG. 74).

A substrate 16 is releaseably mounted to a carrier ring 402, such as by a flexible tape 404 (*e.g.* such as a ring-shaped KAPTON™ tape), whereby the electrical connections 64a-64n (*e.g.* such as seen in Figure 71) on the connector surface 62b of the substrate 16 are aligned to the alignment pins 406, such that the electrical connections 64a-64n on the connector surface 62b of the substrate 16 may be aligned to the conductive pads 284a-284n (FIG. 57) on the lower surface of the system board 282.

The wafer chuck 306 preferably includes a wafer loading vacuum circuit 386, having one or more wafer loading holes 408 on a wafer loading surface 409. The wafer loading vacuum circuit 386 is connectable to a vacuum source 410, and may be sealed by wafer loading vacuum circuit valve 412. A wafer to be tested 304 is placed onto the wafer chuck 306, and is held in place by a applied vacuum applied through the wafer loading holes 408.

A substrate 16, mounted on a carrier ring 402, which is to be mounted to the wafer chuck 306, is controllably positioned over the wafer 104, which is held in place by vacuum applied to the wafer chuck 306. The substrate 16 and the integrated circuit dies 44 are then accurately aligned, such as by a lookup/lookdown camera 414 within a modified wafer probe system 416, whereby the probe springs 61a-61n on the probe surface 62a (FIG. 57) of the substrate 16 are brought into alignment with the die pads 47 on the integrated circuit dies 44. Alignment is typically achieved, either by looking at spring tips 24 (FIG. 2), or at alignment marks 77 (FIG. 14) printed on the substrate 16.

The wafer chuck 306 also preferably includes a carrier ring vacuum circuit 418, having one or more carrier ring vacuum holes 420. The carrier ring vacuum circuit 418 is also connectable to a vacuum source 410, and may be sealed by carrier ring vacuum circuit valve 422. Once the substrate 16 and the integrated circuit dies 44 to be tested are accurately aligned, the lookup/lookdown camera 414 is removed, and the carrier ring 402

is controllably moved onto the wafer chuck 304, whereby the substrate 16 is accurately positioned over the wafer 104, such that the probe springs 61a-61n on the probe surface 62a of the substrate 16 contact the die pads 47 on the integrated circuit dies 44. The carrier ring 402 is held in place by a vacuum applied through the carrier ring vacuum holes 420.

The wafer loading vacuum circuit valve 412 and the carrier ring vacuum circuit valve 422 are then closed, such that the applied vacuum to the wafer loading vacuum circuit 406 and the carrier ring vacuum circuit 418 is maintained, while the entire test assembly can be handled as a unit, for mounting to the system board 282 and test electronics modules 292a-292k. In alternate embodiments of the wafer loading vacuum circuit 406 and the carrier ring vacuum circuit 418, a single valve is used to apply a sealable vacuum to both vacuum circuits 406,418. To enhance the vacuum sustaining ability after the vacuum circuit valves 412 and 422 are closed, each circuit 406,418 preferably includes a vacuum chamber, which serves to maintain the vacuum level over time.

Figure 74 is a second partial expanded cross-sectional view showing massively parallel test assembly and alignment hardware and procedures 424, whereby a massively parallel interface test assembly 278 may be assembled into a system which may then be used for wafer testing. As described above, the system board 282 preferably includes a means for alignment 426 to the carrier ring and/or to the wafer chuck 306, such as alignment holes 426. The system board 282, which is mounted to the test electronics modules 292a-292k and the frame 302, is then positioned over the carrier ring 402, such that the alignment pins 406 engage the alignment holes 426. A means for attachment 428 is then typically provided, such as between the frame 302 and the wafer chuck 306 or the carrier ring 402, thus completing the assembly structure.

While accurate means (*e.g.* such as optical alignment) is typically used to align the fine pitch probe springs 61a-61n to the fine pitch pads 47 on the integrated circuit dies 44 to be tested, the mechanical alignment provided between the carrier ring 402 and the system board 282 (*e.g.* such as between alignment pins 406 and holes 426) is typically sufficient for the distributed electrical connections 64a-64n and pads 284a-284n, which preferably have larger features, and preferably have coarser pitches 322,324, respectively. As well, the flex circuit pitch 334 on the pad matrix is relatively large (*e.g.* on the order of 1 mm), making alignment between the test electronics modules 292a-292k and the system card 282 relatively easy using similar conventional mechanical alignment techniques.

Tester Electronics. Figure 75 is a partial schematic block diagram of test circuitry 430 for the massively parallel interface test systems 278. The tester electronics 430 consists of but not limited to a control computer 432, a power subsystem, test electronics modules 292a-292k, DC parametric and measurement systems 436,438, and control electronics.

As seen in Figure 75, a test electronics module 292 is typically connected to a group 464 of one or more integrated circuit dies 44,100 to be tested which are mounted on a compliant carrier 115, *e.g.* such as but not limited to a column 339 of devices under test 44,100.

The test electronics modules 292a-292k each provide stimulus signals 450 to the devices under test (DUT) 44,100, monitor the responses 454, and store the device under test pass or fail information 458 within the tester memory, or transfer the device under test pass or fail information 458 to the system controller 432.

For example, in memory testing, a test electronics module 292 has all the critical functions of a memory tester. This includes the hardware pattern generator 446 to drive the memory devices under test 44,100 connected to the same test electronics module 292, in parallel. Response detection and fail detection circuits in the test electronics module 292 records the fail locations for each device under test 44,100, as needed.

The test electronics modules 292 are preferably software re-configurable and programmable, making it possible to configure the test electronics modules 292 for a specific DUT design or test function. A built-in self-test (BIST) engine can also be integrated into the test electronics modules 292, such as to provide additional test features.

Each test electronics module 292 also provides analog multiplexing functions, to route the intended DUT pin 47 to the digital test electronics in the test electronics module 292, or to one or more DC measurement subsystems 438, which perform analog measurements of the output signals 454.

Sample Test Sequence. After the carrier-mounted integrated circuit dies 44,100 to be tested are loaded, aligned, and engaged, the system controller 432 sends a control signal to all the power control modules 300, to connect all power and ground pins 47 for a device under test (DUT) 44,100 to ground, except for a selected pin 47 to be tested, which is controllably connected to the DC parametric unit 436. The power supplies 434a-434h are disconnected from the power buses 298a-298h. The power pin

integrity of the selected device 44,100 is then determined, through the DC parametric unit 436.

The DC parametric unit 436, which is connected to the power rails 298a-298h, via relay or solid state switches 435, is then programmed, to check for power to ground shorts. The same sequence is repeated for every power pin on every device under test 44,100.

Similar testing is performed on the DUT input and output pins 47, through the test electronics card 294, to determine short circuits and open circuits for a selected device under test 44,100. An open connection for a device under test 44,100 is typically detected by the absence of a parasitic diode in the input and output pins 47 of the device under test 44,100, as is commonly practiced in the art.

Upon the completion of setup testing, the integrity of the connections and the status of each device pin 47 is determined, in regard to open or short circuits. An excessive number of measured open circuits for one or more devices under test 44,100 on a wafer carrier 115 may be due to an originally defective wafer 104, to system setup, or to one or more defective devices under test 44,100.

The test circuitry 430 preferably provides diagnostic capabilities, to further diagnose faults. Shorts can be isolated from the power busses 298 and pin test electronics 294, by scanning the appropriate bit control pattern into the power control module 300 and pin test electronics module 292.

The remaining devices to be tested 44,100 can then be powered up, and tested in parallel. Short circuit detection and report circuitry is preferably built into each power control module 300, such that a particular device under test 44,100 may be disconnected, if a short circuit is developed in the device under test while the device 44,100 is tested. Other features, such as but not limited to transient device current testing circuitry, may preferably be included within the power control module 300, such as to provide additional test coverage.

Power Pin Testing. The system controller 432 selectively switches on the power connections to one or more devices under test 44,100. With the power supplies 434a-434h turned off (disconnected), a device under test 44,100 can be tested for open circuits and short circuits, using the DC parametric unit 436.

I/O Pin Testing. Similarly, the input and output pins 47 on a device under test 44,100 can be tested for leakage, open, shorts, through the system controller 432.

Device Functional Testing. With test results from power pin testing and I/O pin testing, for any devices under test 44,100 which have failed (*e.g.* due to power), the input and output pins 47 for the failed devices 44,100 are typically isolated from the tester common resources. The remaining devices under test 44,100 which have passed power pin testing and I/O pin testing are then powered up, and may then be tested in parallel.

Functional Testing. The stimulus unit 448 and pattern generator 446 generate the input pattern 450 to the device under test 44,100. The DUT response 454 is captured in the response block 456, which compares the device under test 44,100 output with the expected value from the pattern generator 446 or stimulus unit 448. A pattern generator 446 is commonly used in memory testing, whereas a truth table representing the device stimulus 450 and expected response 454 can be stored in the pattern memory of the stimulus unit 448 for logic device testing. A fail map or log 458 is maintained for each die 44,100. While Figure 75 portrays one embodiment of the functional schematic of the pattern generation and stimulus/response system architecture, other pattern generation and stimulus/response system architectures may suitably be used to meet the testing requirements of a device under test 44, as is commonly practiced in the art.

Alternate Interface Embodiments. Figure 76 is a partial cutaway assembly view of a massively parallel interface assembly 470a, in which a plurality of interface modules 472a-472j are electrically connected to a system interconnect board 486a. Each of the interface modules 472 (*e.g.* such as 472a) includes a pad matrix 288 of electrical conductors 319, which are each electrically connected to a probe spring interposer 476.

Each of the probe spring interposers 476 includes lower surface spring probes 480, electrically connected to upper surface spring probes 484 by vias 482. As described above, the lower surface spring probes 480, as well as the upper surface spring probes 484, may have a variety of tip geometries, such as single point springs 14, interleaved springs 34, or shoulder point springs 50, and are fabricated on the substrate 16, typically using thin-film or MEMS processing methods, to achieve low manufacturing cost, well controlled uniformity, very fine pad pitches 20, and large pin counts. In some embodiments, the flexible connections lower surface spring probes 480 and/or the upper surface spring probes 484 are built in compliance to photolithographic springs,

such as described above, or as disclosed in either U.S. Patent No. 5,848,685 or U.S. Patent No. 5,613,861, which are incorporated herein by reference.

The probe spring interposers 476 are provide electrical connections between each of the interface modules 472a-472j and the system interconnect board 486a. The system interconnect board 486a has upper surface electrical contactors 490, vias 491, upper surface interconnection structures 492 and lower surface interconnection structures 492 494, such that one or more pads one each interface modules 472 may typically be connected together. The system interconnect board 486a may also preferably include board electrical componentry, which may be electrically connected to one or more of the interface modules 472. Each of the interface modules 472 includes links 296 which provide electrical connections to the system interconnect board 486a, and may also preferably include interface module circuitry 498.

Figure 77 is a partial cutaway assembly view of an alternate massively parallel interface assembly 470b, in which a plurality of interface modules 472a-472j are electrically connected, through a system board interposer 500 to a system interconnect board 486b, which includes flexible probe spring 64a-64n, as described above. The system board interposer 500 may preferably include interconnection structures 502 and/or board electrical componentry 504, which may be electrically connected to one or more of the interface modules 472.

The massively parallel interface assemblies 470a,470b each provide a versatile and robust interface between a plurality of interconnected structures. The massively parallel interface assembly 470a may simply be used to provide a robust massively parallel interface, such as to provide complex parallel connections between similar components. In preferred interface embodiments, the massively parallel interface assemblies 470a,470b may also include module specific electronic circuitry 498, or shared circuitry 496.

Figure 78 is a schematic block diagram 506 of connections between a plurality of computer systems 508a-508n, using a massively parallel interface assembly 470. Figure 79 is a schematic block diagram 510 of connections between a plurality of electronic circuits 512a-512n, using a massively parallel interface assembly 470.

System Advantages. The massively parallel interface assemblies 278a-278d provide signal and power interconnections between a test system and a large number of devices 44,100 located on a wafer carrier 115, while providing planarity compliance between the integrated circuits 44,100 and successive assembly layers (*e.g.* such as

the system board 282 and the pad matrices 288 on the test electronics modules 292a-292k.

As well, the massively parallel interface assemblies 278a-278d provide short electrical paths for the power and input and output signals, between the test electronics modules 292a-292k and the devices under test 44,100, through the combined use of the system board 282 and the vertically packaged test electronics modules 292a-292k, which typically include flex circuits 290.

Furthermore, while the massively parallel interface assemblies 278a-278d provide short electrical paths for the power and input and output signals, between the test electronics modules 292a-292k and the devices under test 44,100 (thereby reducing round trip transit time), the massively parallel interface assemblies 278a-278d provide thermal isolation between the test electronics 294 and the devices under test 44,100, such that the devices under test 44,100 may be controllably operated over a wide temperature range, while the test electronics modules 292a 292k provide enhanced heat transfer away from heat sensitive components (*e.g.* such as through buss bars 298a-298h), and while preferably providing enhanced test module temperature control.

As described above, the massively parallel test interface assemblies 278 may be used to detect power to ground shorts in any die quickly, and to isolate power from a die having a detected power to ground short before damage is done to the test electronics. In addition, the massively parallel test interface assemblies 278 and related test system may be used to detect that the contacts to many, hundreds, or even hundreds of thousands of pads are reliably made and whether each of the contacts are within the contact resistance specification, and to assure that the self inductance and self capacitance of each signal line are below values that would adversely affect test signal integrity.

Furthermore, the massively parallel test interface assemblies 278 and related test system can be used to detect whether the mutual inductance and mutual capacitance between pairs of signal lines and between signal lines and power or ground lines are below values that would adversely affect test signal integrity.

As well, the massively parallel test interface assemblies 278 provide stimulus and response detection and analysis to many, hundreds, or even thousands, of die under test in parallel, and which preferably provides diagnostic tests to a failed die, in parallel with the continued testing of all other die.

In addition, the massively parallel test interface assemblies 278 can reliably and repeatedly establish contact to many, hundreds, or even thousands of pads 47, without the need to periodically stop and inspect and/or clean the probe interface structure 16.

Furthermore, the massively parallel test interface assemblies 278 inherently organize and manage the interconnections between the devices under test 44 and the tester electronics 430, while maintaining signal integrity and power and ground stability, and assures that no two or more adjacent pads 47 are contacted by a single test probe tip.

Although the disclosed massively parallel interface assemblies are described herein in connection with integrated circuit testing, computer networking, and circuit connections, the assemblies and techniques can be implemented with a wide variety devices and circuits, such as interconnections between integrated circuits and substrates within electronic components or devices, burn-in devices and MEMS devices, or any combination thereof, as desired.

Accordingly, although the invention has been described in detail with reference to a particular preferred embodiment, persons possessing ordinary skill in the art to which this invention pertains will appreciate that various modifications and enhancements may be made without departing from the spirit and scope of the claims that follow.

CLAIMS

What is claimed is:

1. An apparatus, comprising:

an integrated circuit die comprising a substrate having a first surface and a second surface, and integrated circuit, and a plurality of integrated circuit contacts located on the first surface and electrically connected to the integrated circuit;

a plurality of stress metal springs electrically connected to the integrated circuit contacts, the plurality of stress metal springs comprising a plurality of metal layers at least two of the metal layers having different initial levels of stress, the stress metal springs defining a loop structure which is rotated by an effective rotation angle away from the first surface of the integrated circuit; and

a polymer layer substantially covering the first surface of the integrated circuit and a portion of each of the plurality of stress metal springs, such that a portion of the loop structure of each of the plurality of stress metal springs extends beyond the polymer layer.

2. The apparatus of Claim 1, wherein the at least two of the metal layers are comprised of the same metal and have an initial stress gradient.

3. The apparatus of Claim 1, wherein each of the plurality of stress metal springs further comprises at least one plating layer which substantially covers the loop structure.

4. The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises nickel.

5. The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises a nickel alloy.

6. The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises gold.

7. The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises silver.

8. The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises rhodium.

9. The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises palladium.

10. The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises cobalt.

11. The apparatus of Claim 1, wherein the polymer layer comprises an elastomer.

12. The apparatus of Claim 1, wherein the plurality of integrated circuit contacts comprise contact pads.

13. The apparatus of Claim 1, wherein the effective rotation angle is less than 90 degrees.

14. The apparatus of Claim 1, wherein the effective rotation angle is greater than 180 degrees.

15. The apparatus of Claim 1, wherein the effective rotation angle is approximately 270 degrees.

16. The apparatus of Claim 1, wherein the first metal layer of the plurality of metal layers of the each of the plurality of stress metal springs which is directly connected to the integrated circuit and forms the outer convex layer on the loop structure is a boundary layer.

17. The apparatus of Claim 1, wherein the boundary layer comprises gold.

18. The apparatus of Claim 1, wherein the boundary layer comprises rhodium.

19. The apparatus of Claim 1, wherein the boundary layer comprises palladium.

20. The apparatus of Claim 1, wherein the portion of the loop structure of each of the plurality of stress metal springs which extends beyond the polymer layer further comprises an expanded contact surface.

21. An apparatus, comprising:

a compliant wafer carrier substrate having a first surface and a second surface; and

a plurality of chip scale packages adhesively attached to the first surface of the compliant wafer carrier;

each of the plurality of chip scale packages comprising an integrated circuit die comprising a substrate having a first surface and a second surface, an integrated circuit device, and a plurality of integrated circuit contacts located on the first surface and electrically connected to the integrated circuit device.

22. The apparatus of Claim 21, wherein each of the plurality of chip scale packages further comprise:

a plurality of stress metal springs electrically connected to the integrated circuit contacts, the plurality of stress metal springs comprising a plurality of metal layers, at least two of the metal layers having different initial levels of stress, the stress metal springs defining a loop structure which is rotated by an effective rotation angle away from the first surface of the integrated circuit due to the different initial levels of stress, and a polymer layer substantially covering the first surface of the integrated circuit and a portion of each of the plurality of stress metal springs, such that a portion of the loop structure of each of the plurality of stress metal springs extends beyond the polymer layer.

23. An interposer, comprising:

a electrically insulative support substrate having a first surface and a second surface; and

at least one stress metal spring extending at least from the first surface to the second surface of the support substrate, each of the at least one stress metal spring comprising a plurality of metal layers, at least two of the metal layers having different levels of stress, each of the at least one stress metal spring defining a loop structure which is rotated by an effective rotation angle away from the first surface of the support substrate.

24. The interposer of Claim 23, wherein the support substrate comprises a polymer.

25. The interposer of Claim 23, wherein the support substrate comprises an elastomer.

26. The interposer of Claim 23, wherein the at least two of the metal layers are comprised of the same metal and have an initial stress gradient.

27. A process, comprising the steps of:

providing a sacrificial substrate;

establishing a plurality of metal layers on the sacrificial substrate, at least two of the metal layers having different levels of stress;

releasing a portion of the plurality of metal layers to form a non-planar loop structure which is rotated by an effective rotation angle away from the sacrificial substrate;

establishing a polymer layer over the sacrificial substrate, the plurality of metal layers, and the formed non-planar loop structure;

removing a portion of the established polymer layer to expose a portion of the formed non-planar loop structure; and

removing the sacrificial substrate.

28. The process of Claim 27, wherein the at least two of the metal layers are comprised of the same metal and have an initial stress gradient.

29. The process of Claim 27, wherein the first of the established plurality of metal layers comprises a boundary layer.

30. The process of Claim 29, wherein the boundary layer comprises gold.

31. The process of Claim 29, wherein the boundary layer comprises rhodium.

32. The process of Claim 29, wherein the boundary layer comprises palladium.

33. The process of Claim 27, further comprising the step of:

forming at least one plated layer over the non-planar loop structure.

34. The process of Claim 33, wherein at least one of the at least one formed plated layer comprises nickel.

35. The process of Claim 33, wherein at least one of the at least one formed plated layer comprises a nickel alloy.

36. The process of Claim 33, wherein at least one of the at least one formed plated layer comprises gold.

37. The process of Claim 33, wherein at least one of the at least one formed plated layer comprises rhodium.

38. The process of Claim 33, wherein at least one of the at least one formed plated layer comprises palladium.

39. The process of Claim 33, wherein at least one of the at least one formed plated layer comprises cobalt.

40. The process of Claim 27, wherein the sacrificial substrate further comprises a groove at least one groove.

41. The process of Claim 27, wherein the sacrificial substrate further comprises a groove, further comprising the step of:

filling the groove with an electrically conductive material;

wherein a portion of the plurality of metal layers is established on the electrically conductive material.

42. The process of Claim 27, wherein the established polymer layer comprises a plurality of polymer layers.

43. The process of Claim 27, wherein the effective rotation angle is less than 90 degrees.

44. The process of Claim 27, wherein the effective rotation angle is greater than 180 degrees.

45. The process of Claim 27, wherein the effective rotation angle is approximately 270 degrees.

46. A contactor, comprising:

a substrate having a first surface and a second surface, and a plurality of conductive vias extending from the first surface to the second surface;

a plurality of stress metal springs electrically connected to the vias, the plurality of stress metal springs comprising a plurality of metal layers, at least two of the metal layers having different initial levels of stress, the stress metal springs defining a loop structure which is rotated by an effective rotation angle due to the different initial levels of stress away from the first surface of the substrate, wherein each of the plurality of stress metal springs further comprises a primary plating layer which substantially covers the loop structure.

47. The contactor of Claim 46, wherein the primary plating layer comprises nickel.

48. The contactor of Claim 46, wherein the primary plating layer comprises a nickel alloy.

49. The contactor of Claim 46, wherein the primary plating layer comprises cobalt.

50. The contactor of Claim 46, further comprising a secondary plating layer over the primary plating layer.

51. The contactor of Claim 50, wherein the secondary plating layer comprises rhodium.

52. The contactor of Claim 50, wherein the secondary plating layer comprises gold.

53. A contactor, comprising:

a substrate having a first surface and a second surface, and a plurality of conductive vias extending from the first surface to the second surface;

a plurality of stress metal springs electrically connected to the vias, the plurality of stress metal springs comprising a plurality of metal layers, at least two of the metal layers having different initial levels of stress, the stress metal springs defining a loop structure which is rotated by an effective rotation angle due to the different initial levels of stress away from the first surface of the substrate; and

a polymer layer substantially covering the first surface of the substrate and a portion of each of the plurality of stress metal springs, such that a portion of the loop structure of each of the plurality of stress metal springs extends beyond the polymer layer.

54. The contactor of Claim 53, wherein the at least two of the metal layers are comprised of the same metal and have an initial stress gradient.

55. The contactor of Claim 53, wherein each of the plurality of stress metal springs further comprises at least one plating layer which substantially covers the loop structure.

56. The contactor of Claim 55, wherein at least one of the at least one plating layer comprises nickel.

57. The contactor of Claim 55, wherein at least one of the at least one plating layer comprises a nickel alloy.

58. The contactor of Claim 55, wherein at least one of the at least one plating layer comprises gold.

59. The contactor of Claim 55, wherein at least one of the at least one plating layer comprises rhodium.

60. The contactor of Claim 55, wherein at least one of the at least one plating layer comprises palladium.

61. The contactor of Claim 55, wherein at least one of the at least one plating layer comprises cobalt.

62. The contactor of Claim 53, wherein the polymer layer comprises an elastomer.

63. The contactor of Claim 53, wherein the portion of the loop structure of each of the plurality of stress metal springs which extends beyond the polymer layer comprises a contact pad region.

64. The contactor of Claim 53, wherein the effective rotation angle is less than 90 degrees.

65. The contactor of Claim 53, wherein the effective rotation angle is greater than 180 degrees.

66. The contactor of Claim 53, wherein the effective rotation angle is approximately 270 degrees.

67. A process, comprising the steps of:

providing a contactor substrate having a first surface and a second surface, and a conductive via extending from the first surface to the second surface;

establishing a plurality of metal layers on the contactor substrate in electrical contact with the via, at least two of the metal layers having different initial levels of stress;

releasing a portion of the plurality of layers to form a non-planar loop structure which is rotated by an effective rotation angle due to the different initial layers of stress away from the contactor substrate; and

forming the support substrate over the contactor substrate and partially over the formed non-planar loop structure.

68. The process of Claim 67, wherein the step of forming the support substrate over the contactor substrate and partially over the formed non-planar loop structure further comprises:

establishing the support substrate over the contactor substrate, the plurality of metal layers, and the formed non-planar loop structure; and

removing a portion of the established support substrate to expose a portion of the formed non-planar loop structure.

69. The process of Claim 67, wherein effective rotation angle is less than 90 degrees.

70. The process of Claim 67, wherein effective rotation angle is greater than 180 degrees.

71. The process of Claim 67, wherein effective rotation angle is approximately 270 degrees.

72. The process of Claim 67, wherein the first of the established plurality of metal layers comprises a boundary layer.

73. The process of Claim 72, wherein the boundary layer comprises gold.

74. The process of Claim 72, wherein the boundary layer comprises rhodium.

75. The process of Claim 72, wherein the boundary layer comprises palladium.

76. The process of Claim 67, further comprising the step of:

forming at least one plated layer over the non-planar loop structure.

77. The process of Claim 76, wherein at least one of the at least one formed plated layer comprises nickel.

78. The process of Claim 76, wherein at least one of the at least one formed plated layer comprises a nickel alloy.

79. The process of Claim 76, wherein at least one of the at least one formed plated layer comprises gold.

80. The process of Claim 76, wherein at least one of the at least one formed plated layer comprises rhodium.

81. The process of Claim 76, wherein at least one of the at least one formed plated layer comprises palladium.

82. The process of Claim 76, wherein at least one of the at least one formed plated layer comprises cobalt.

83. The process of Claim 67, wherein the contactor substrate further comprises at least one groove.

84. The process of Claim 67, wherein the contactor substrate further comprises a groove, further comprising the step of;

filling the groove with an electrically conductive material;

wherein a portion of the plurality of metal layers is established on the electrically conductive material.

85. The process of Claim 67, wherein the established polymer layer comprises a plurality of polymer layers.

86. A system, comprising:

a compliant carrier having a first surface and a second surface;

at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at least one integrated circuit a plurality of electrical connections on the upper surface;

a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface; and

a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board.

87. The system of Claim 86, wherein the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device are photolithographically patterned springs.

88. The system of Claim 86, wherein the plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board are stress metal springs on the upper surface of each of the at least one integrated circuit device.

89. The system of Claim 86, wherein each of the plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface

of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board are flexible spring probes on the bottom surface of the system board.

90. The system of Claim 89, wherein the flexible spring probes on the bottom surface of the system board are photolithographically patterned springs.

91. The system of Claim 86, further comprising:

a travel limit mechanism which limits perpendicular travel of each of the at least one integrated circuit device in relation to the system board.

92. The system of Claim 86, further comprising:

a pressure plate support;

wherein the second surface of the compliant carrier is supported on the pressure plate support.

93. The system of Claim 92, wherein the pressure plate support is compliant.

94. The system of Claim 86, wherein the compliant carrier is thermally conductive.

95. The system of Claim 86, wherein the compliant carrier is electrically conductive.

96. The system of Claim 86, further comprising:

at least one interface module having a plurality of electrically conductive pads on a planar region, at least one of the electrically conductive pads connected to at least one interconnection region, and at least one link connected to at least one of the at least one interconnection region; and

means for fixedly holding each of the at least one interface module in relation to the system board, such that the plurality of electrically conductive pads on the planar region of each of the at least one interface module contact at least one of the plurality of electrical conductors on the top surface of the system board.

97. The system of Claim 96, wherein each of the at least one interface module includes a circuit having a first surface and a second surface, and wherein the plurality of electrically conductive pads are located on the first surface.

98. The system of Claim 97, wherein the circuit is a flexible circuit.

99. The system of Claim 97, wherein the circuit is a semi-rigid circuit.

100. The system of Claim 97, wherein the circuit is a rigid circuit.

101. The system of Claim 96, further comprising:

at least one buss bar electrically connected to at least one of the at least one interconnection region.

102. The system of Claim 101, further comprising:

at least one power control module located on the at least one interface module, each of the at least one power control module electrically connected between the at least one buss bar and at least one of the at least one the interconnection region.

103. The system of Claim 102, wherein the at least one power control module is in thermal contact with the at least one buss bar.

104. The system of Claim 101, further comprising:

at least one power control module located on the at least one buss bar, each of the at least one power control module electrically connected between the at least one buss bar and at least one of the at least one the interconnection region.

105. The system of Claim 104, wherein the at least one power control module is in thermal contact with the at least one buss bar.

106. A process, comprising the steps of:

providing a compliant carrier having an first surface and a second surface;

adhesively attaching a wafer comprising at least one integrated circuit device lower surface and an upper surface on the first surface of the compliant carrier, each of the at least one integrated circuit having a plurality of electrical connections on the upper surface;

separating each of the at least one integrated circuit devices from the other of the at least one integrated circuit devices;

providing a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface; and

creating a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board.

107. The process of Claim 106, further comprising the steps of:

providing at least one interface module having a plurality of electrically conductive pads on a planar region, at least one of the electrically conductive pads connected to at least one interconnection region, and at least one link connected to at least one of the at least one interconnection region; and

fixedly holding each of the at least one interface module in relation to the system board, such that the plurality of electrically conductive pads on the planar region of each of the at least one interface module contact at least one of the plurality of electrical conductors on the top surface of the system board.

108. The process of Claim 106, further comprising the step of:

providing a pressure plate support; and

supporting the second surface of the compliant carrier on the pressure plate support.

109. The process of Claim 108, wherein the pressure plate support is compliant.

110. The process of Claim 106, wherein the compliant carrier is thermally conductive.

111. The process of Claim 106, wherein the compliant carrier is electrically conductive.

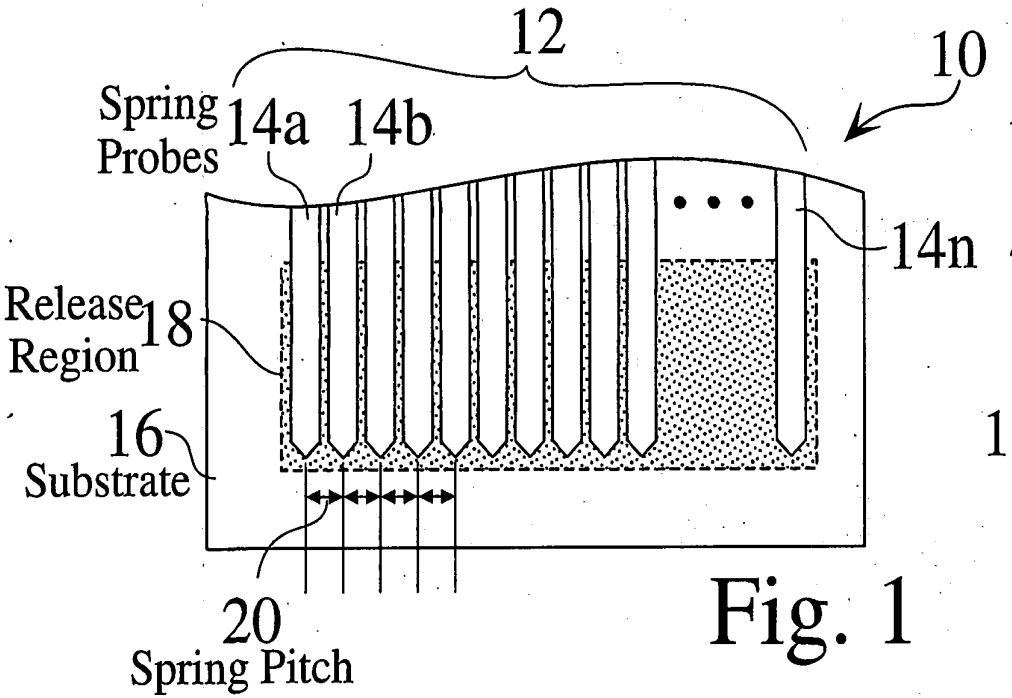


Fig. 1

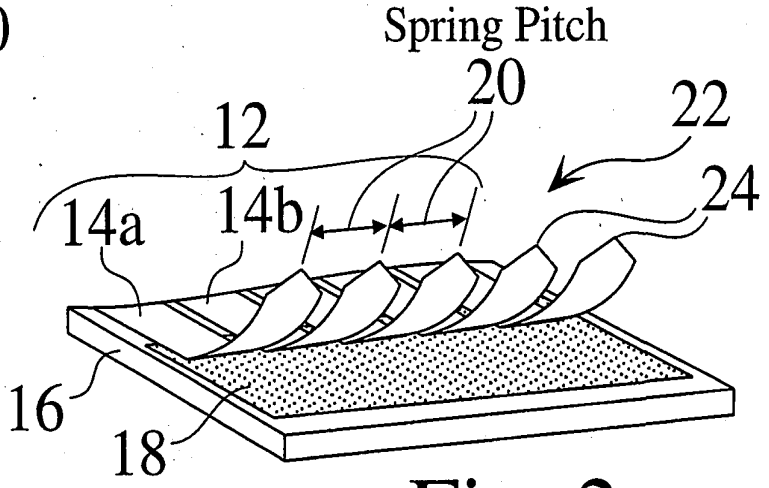


Fig. 2

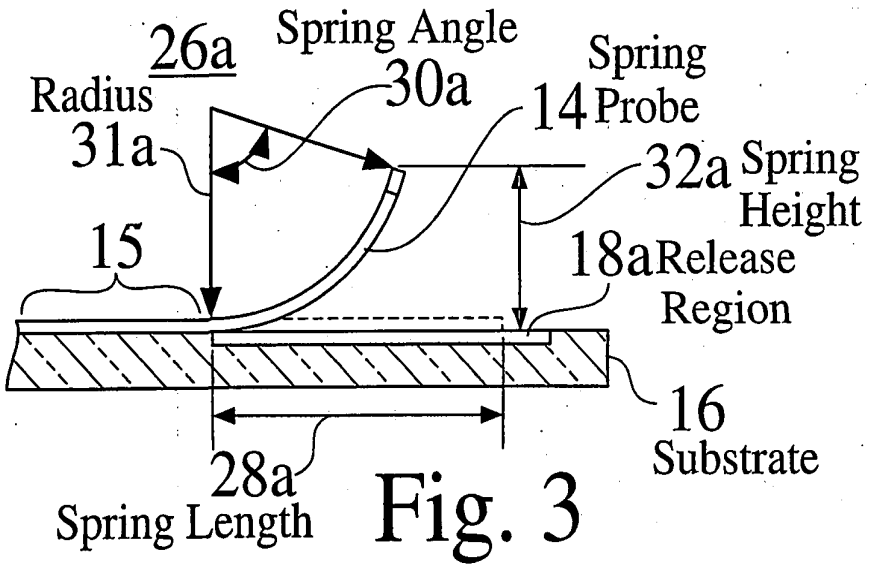


Fig. 3

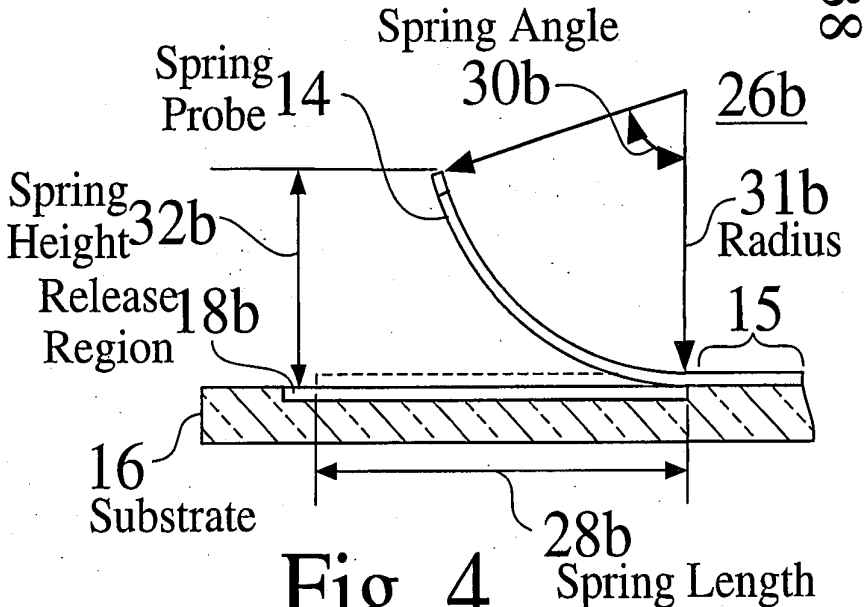


Fig. 4

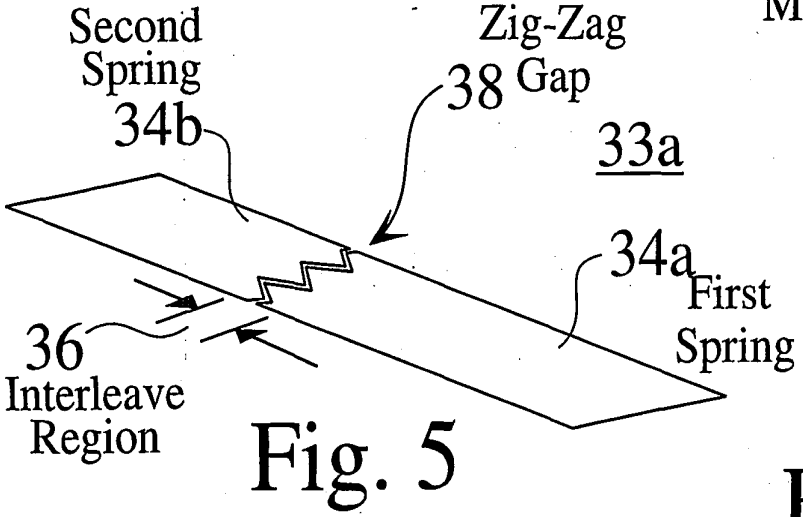


Fig. 5

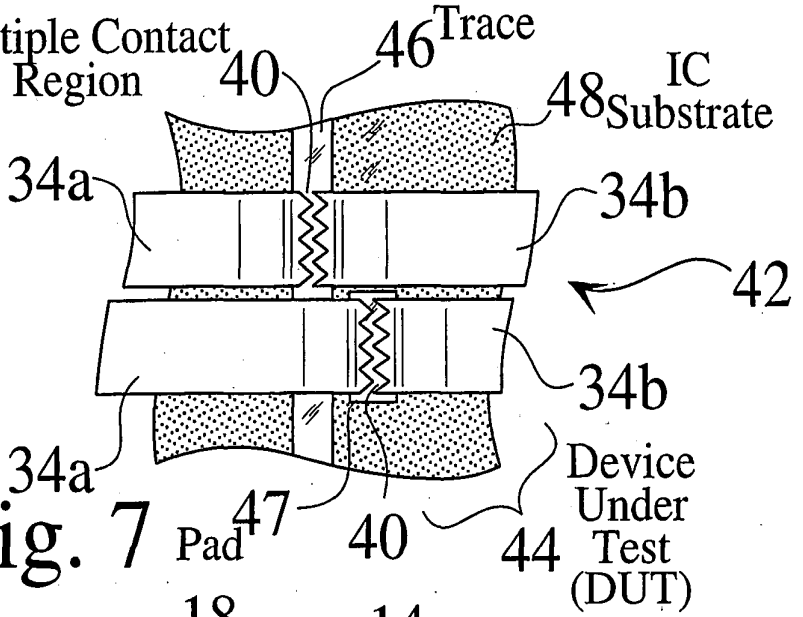


Fig. 7

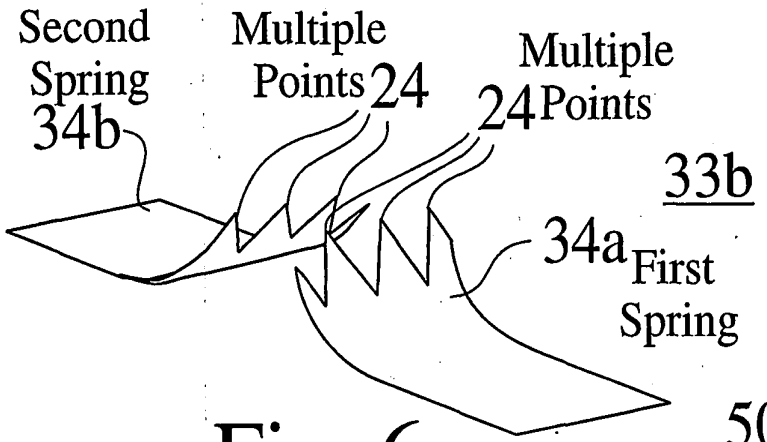


Fig. 6

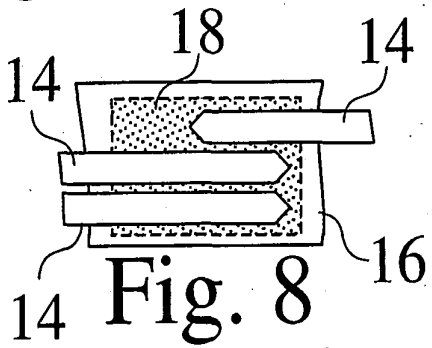


Fig. 8

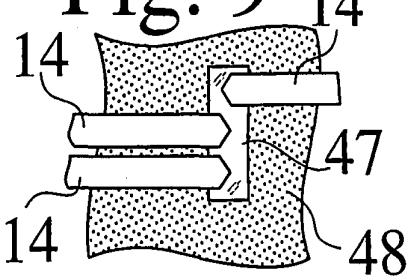


Fig. 9

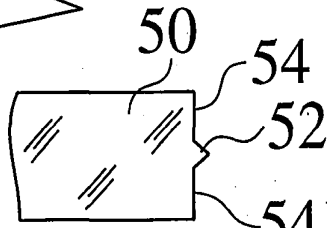


Fig. 10

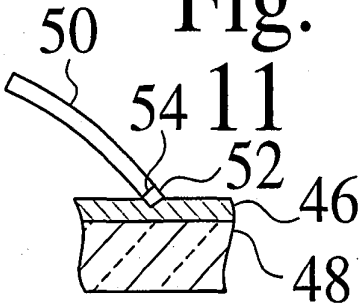


Fig. 11

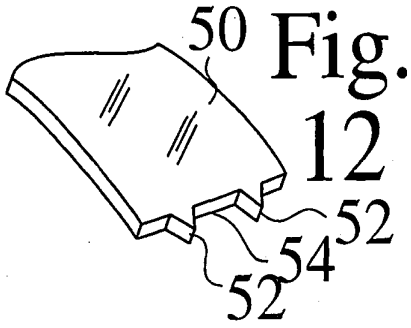


Fig. 12

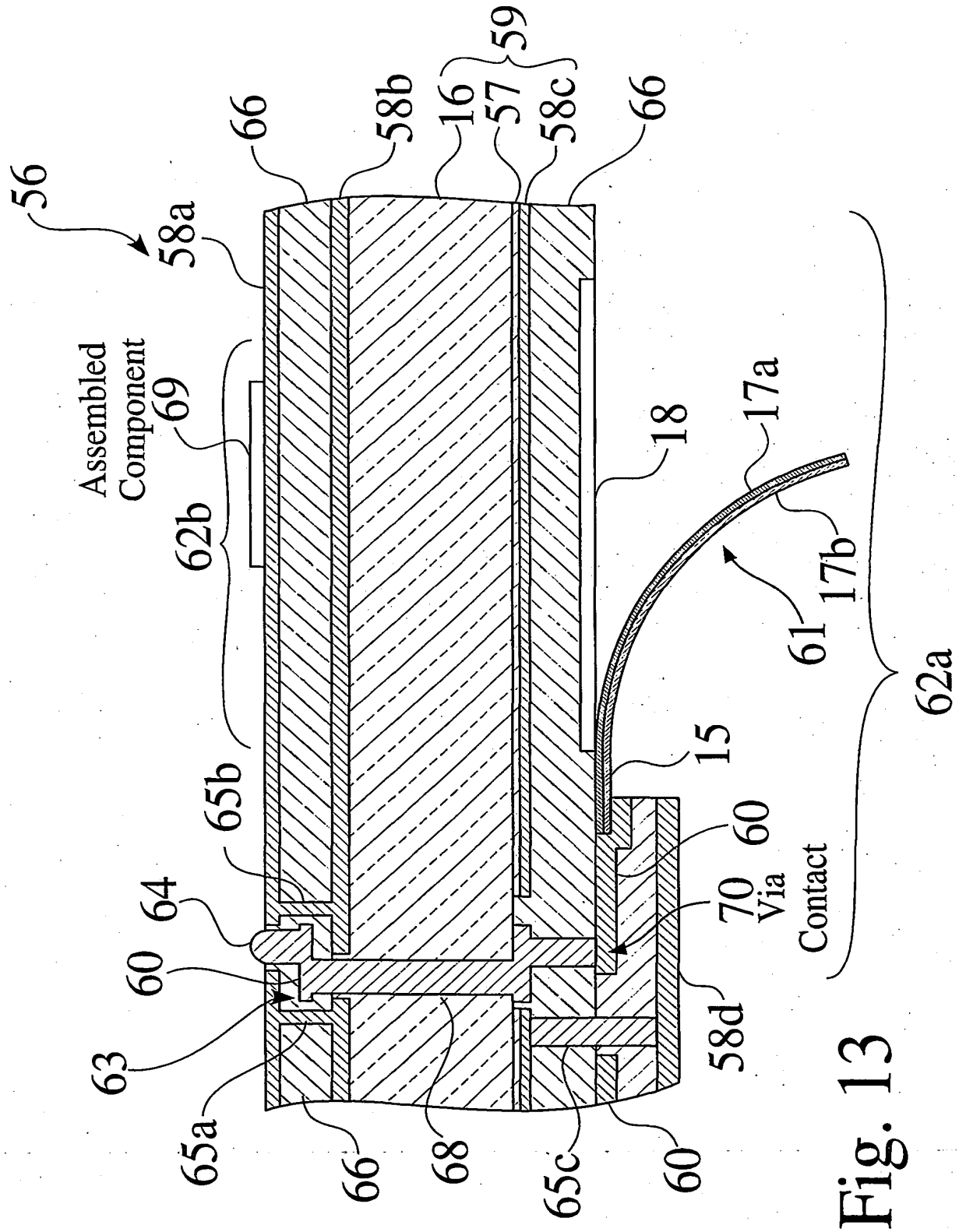

56
58a
66
58b
16
57
58c
59
66
Assembled Component
69
62b
18
17a
17b
61
62a
65b
15
64
60
Via
70
Contact
60
63
58d
65a
66
68
65c
60

Fig. 13

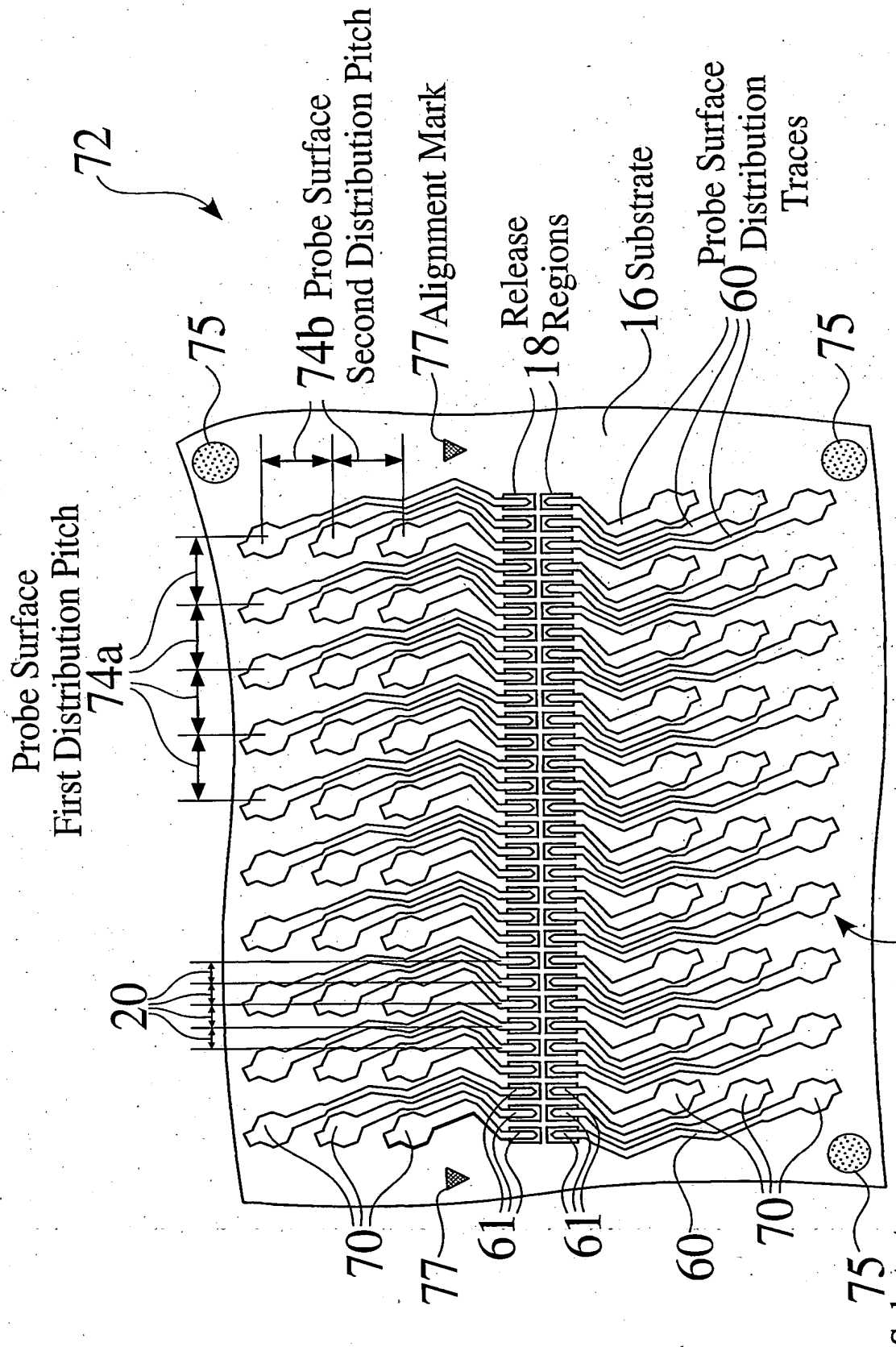

72
Probe Surface
First Distribution Pitch
74a
74b Probe Surface
Second Distribution Pitch
77 Alignment Mark
Release
18 Regions
16 Substrate
Probe Surface
60 Distribution
Traces
75
20
62a
70
77
61
61
60
70
75
Substrate
Standoff

Fig. 14

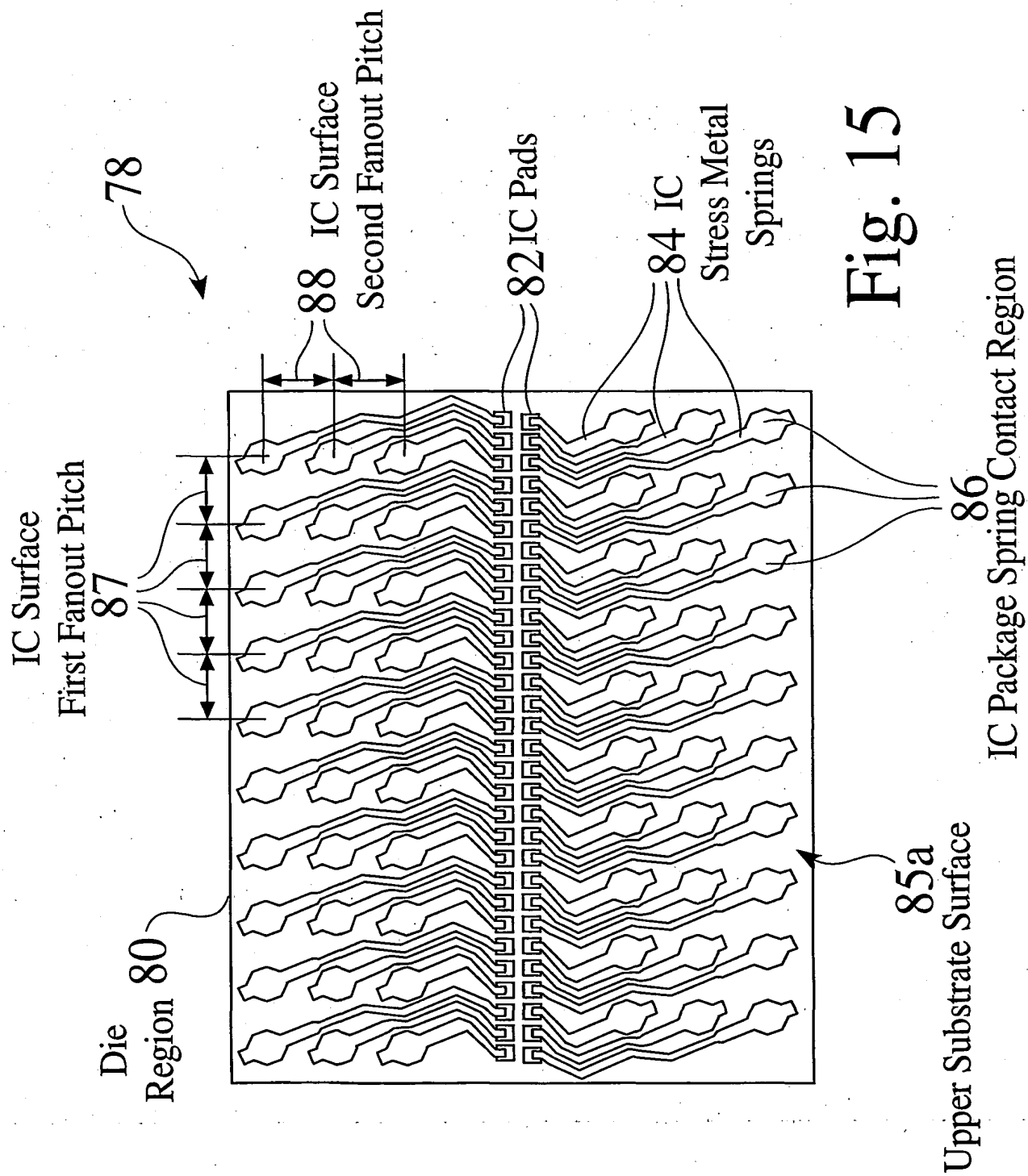

78
88 IC Surface Second Fanout Pitch
82 IC Pads
84 IC Stress Metal Springs
IC Surface First Fanout Pitch 87
86 IC Package Spring Contact Region
Die Region 80
85a Upper Substrate Surface

Fig. 15

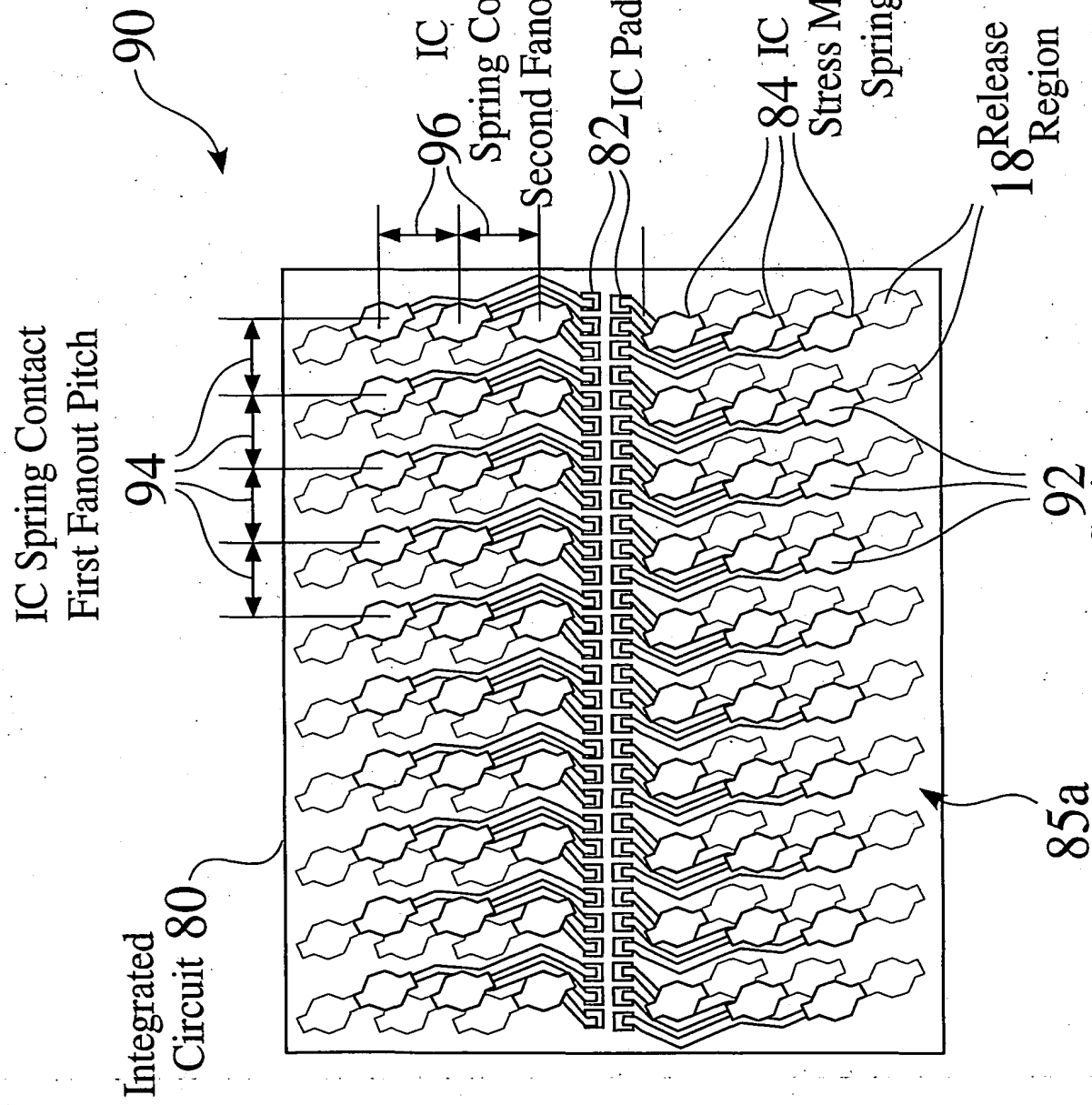

90
IC Spring Contact
First Fanout Pitch
94
96 IC
Spring Contact
Second Fanout Pitch
82 IC Pads
84 IC
Stress Metal
Springs
18 Release
Region
92
Spring
Contact Surface
85a
Integrated
Circuit 80

Fig. 16

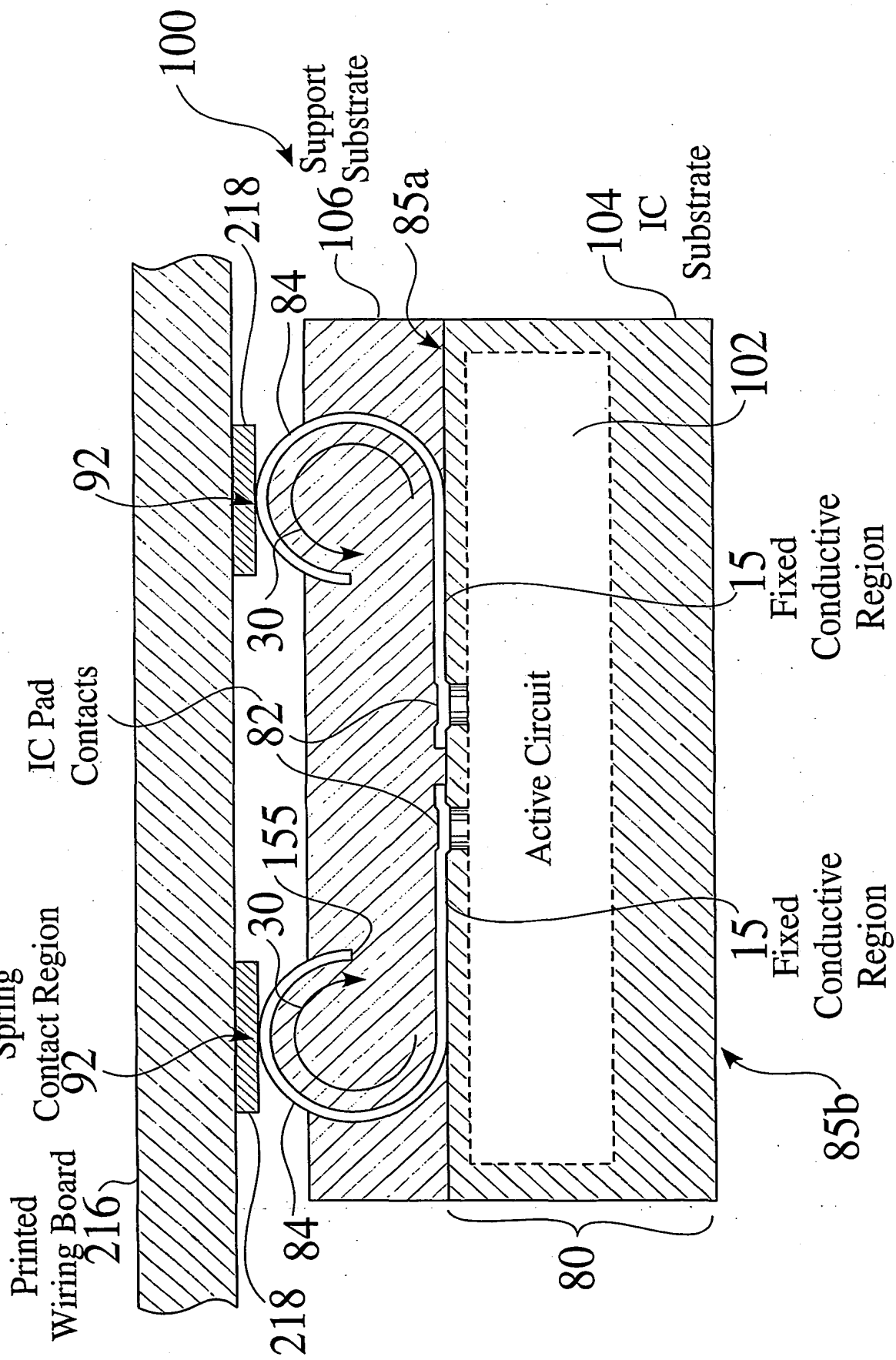

100
Support Substrate
106
218
85a
104
IC Substrate
84
92
102
30
15
Fixed Conductive Region
IC Pad Contacts
82
Active Circuit
155
30
15
Fixed Conductive Region
Spring Contact Region
92
85b
Printed Wiring Board
216
218
84
80

Fig. 17

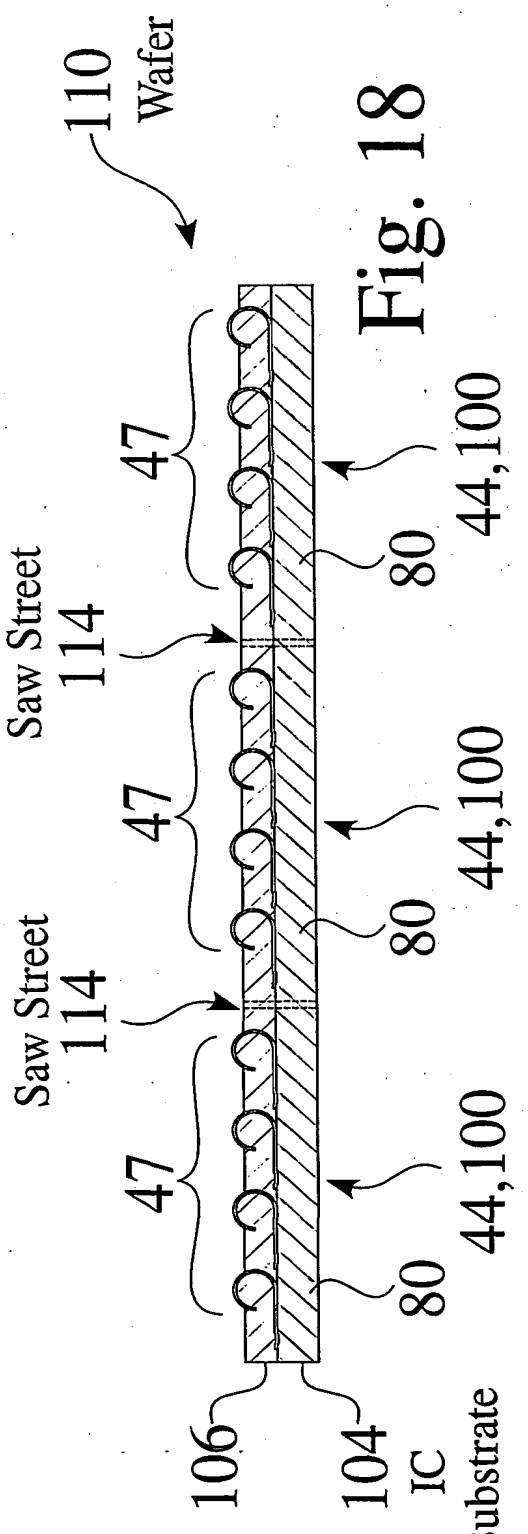

110
Wafer
Saw Street
114
47
80
44,100
106
104
IC
Substrate

Fig. 18

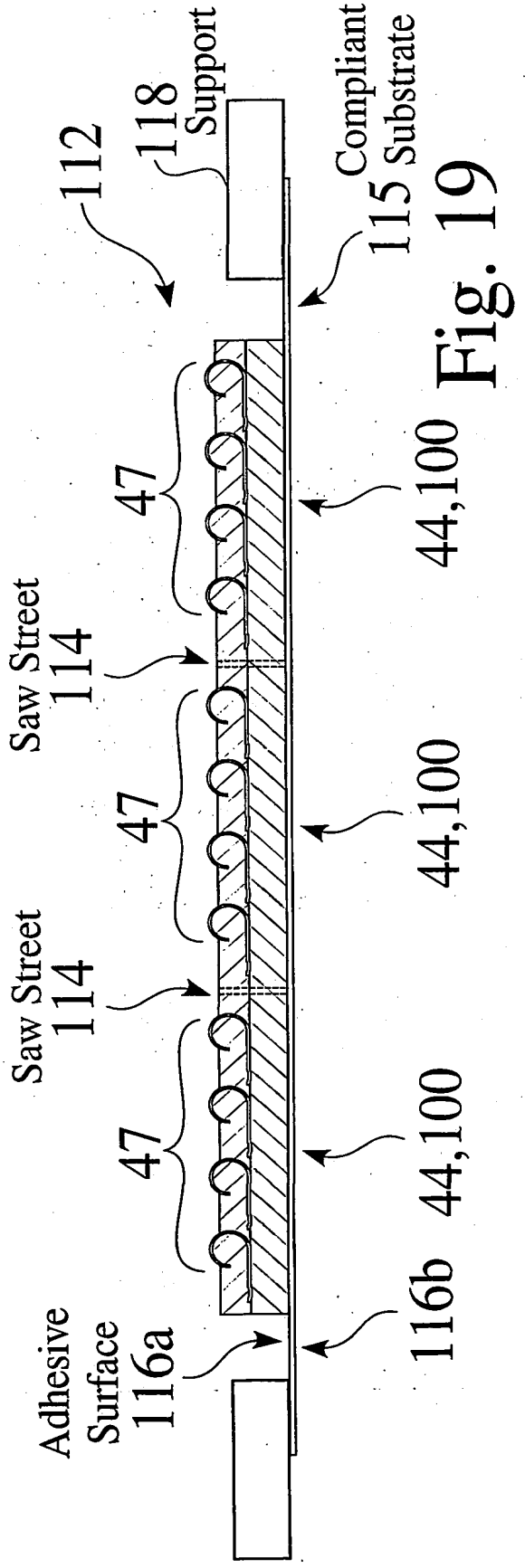

112
118
Support
Compliant
115
Substrate
Saw Street
114
47
44,100
Adhesive
Surface
116a
116b

Fig. 19

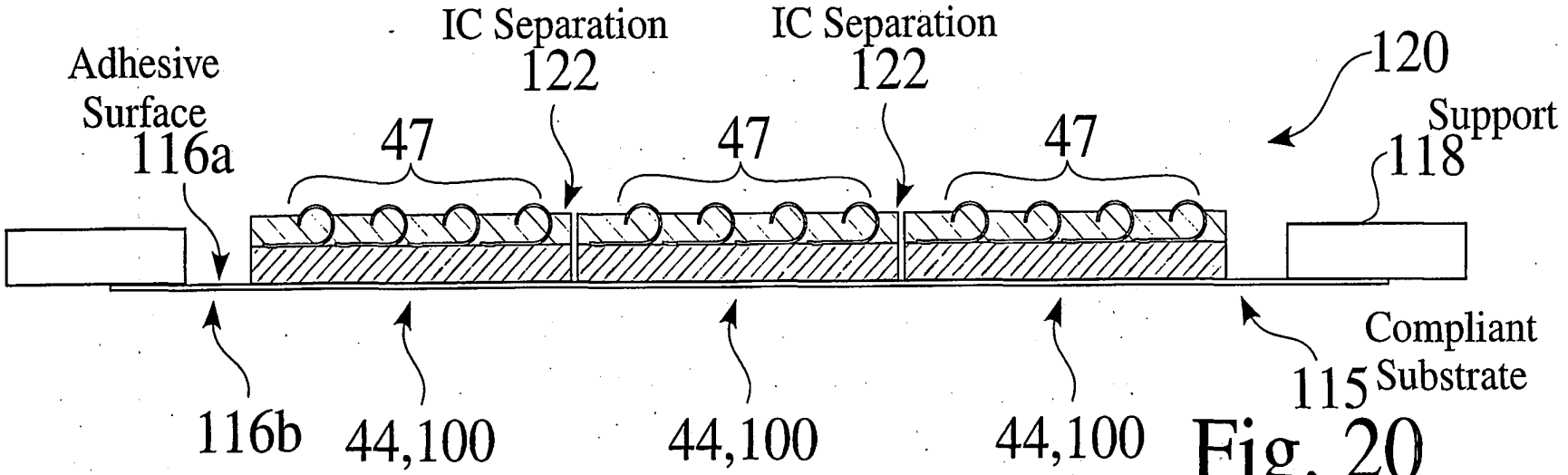

Adhesive Surface
116a
IC Separation
122
IC Separation
122
120
Support
118
47
47
47
Compliant Substrate
115
116b
44,100
44,100
44,100

Fig. 20

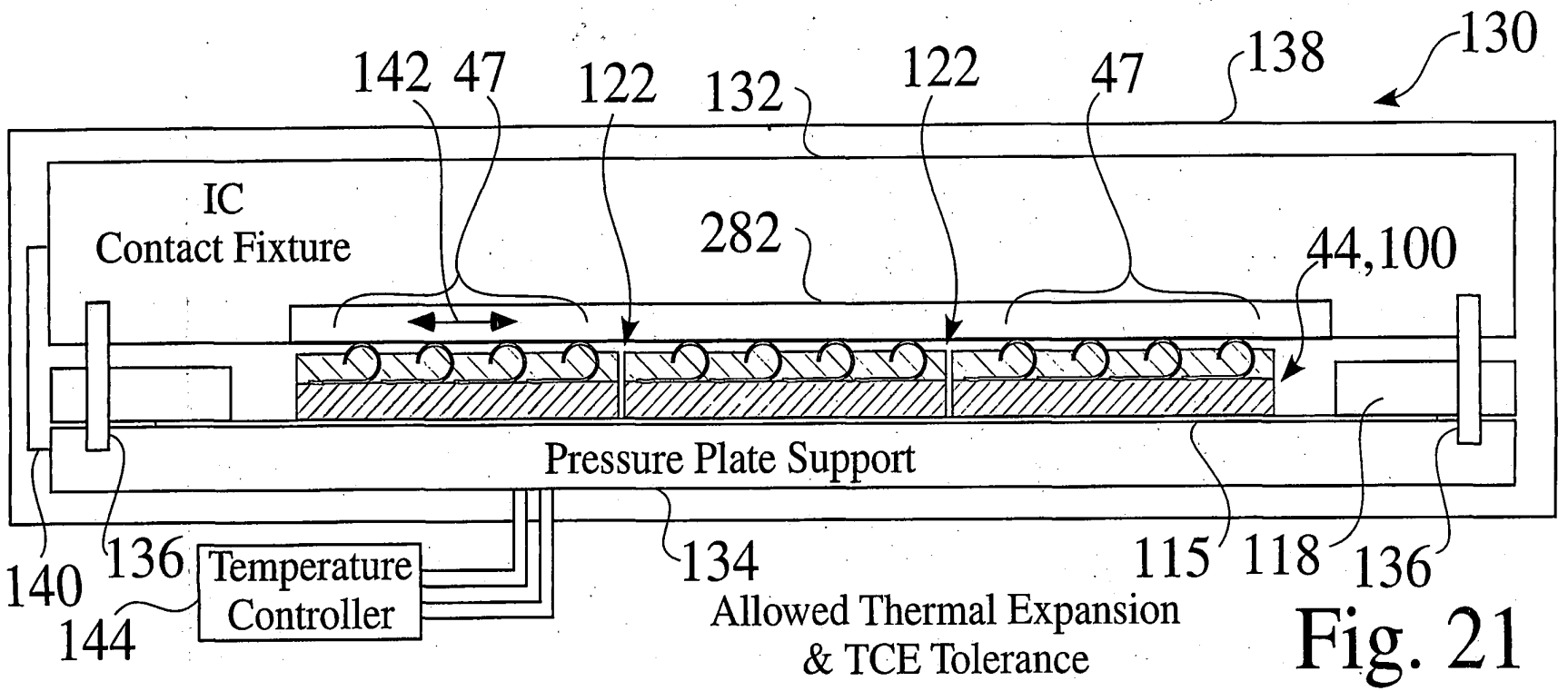

142
47
122
132
122
47
138
130
IC
Contact Fixture
282
44,100
Pressure Plate Support
140
136
Temperature Controller
144
134
Allowed Thermal Expansion & TCE Tolerance
115
118
136

Fig. 21

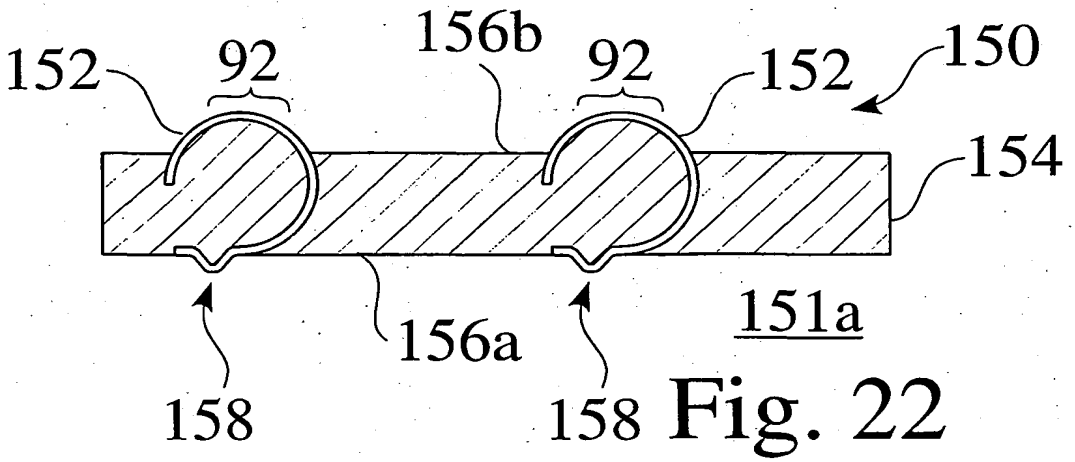


Fig. 22

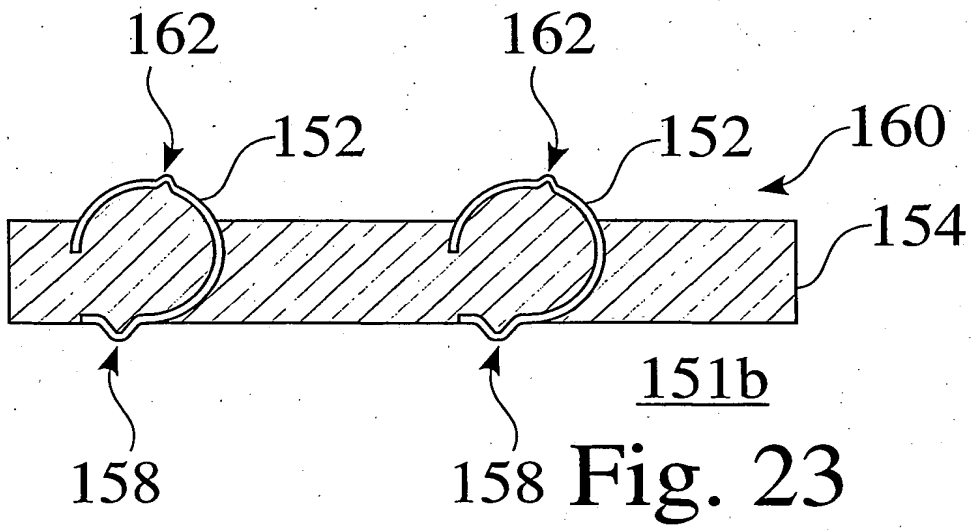


Fig. 23

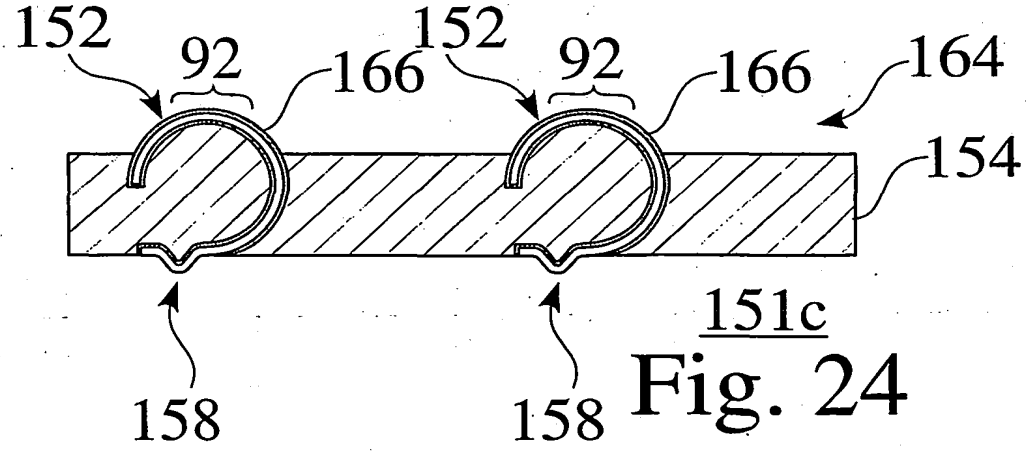


Fig. 24

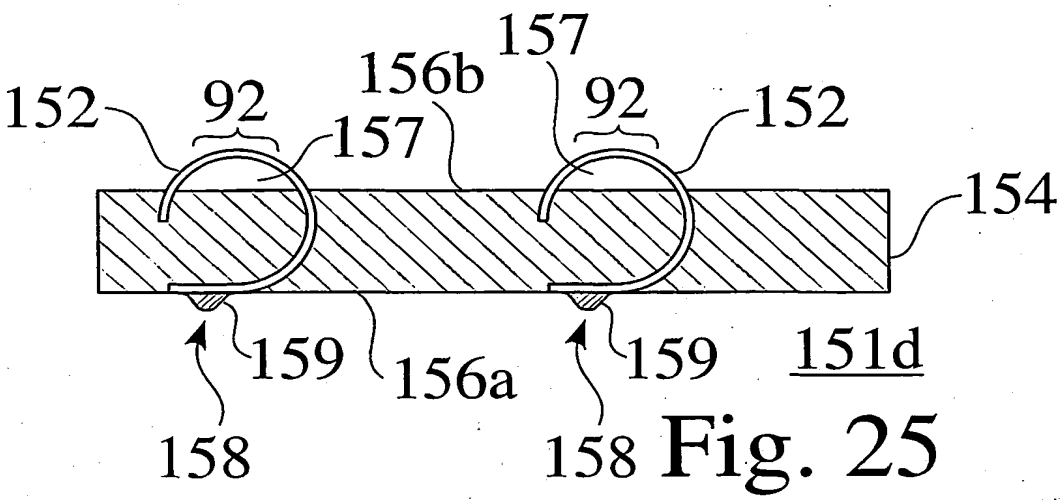


Fig. 25

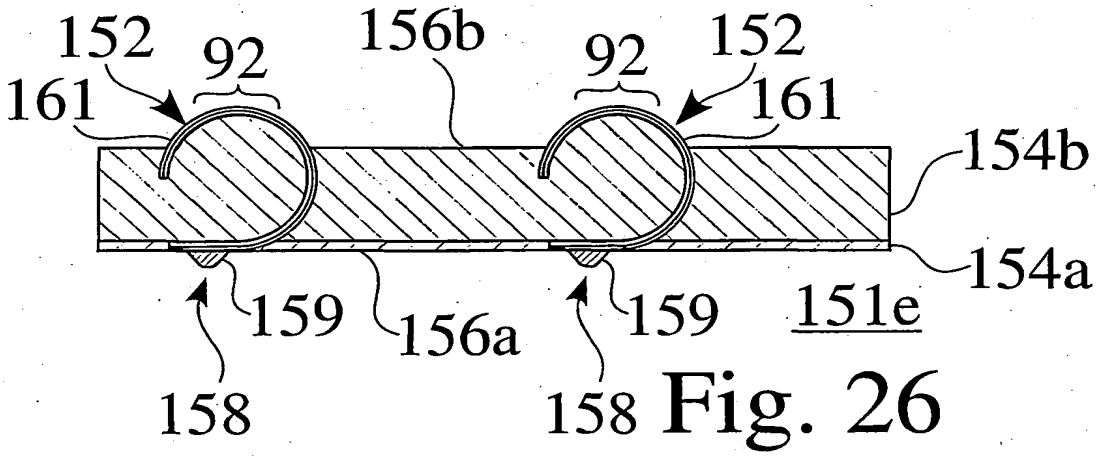


Fig. 26

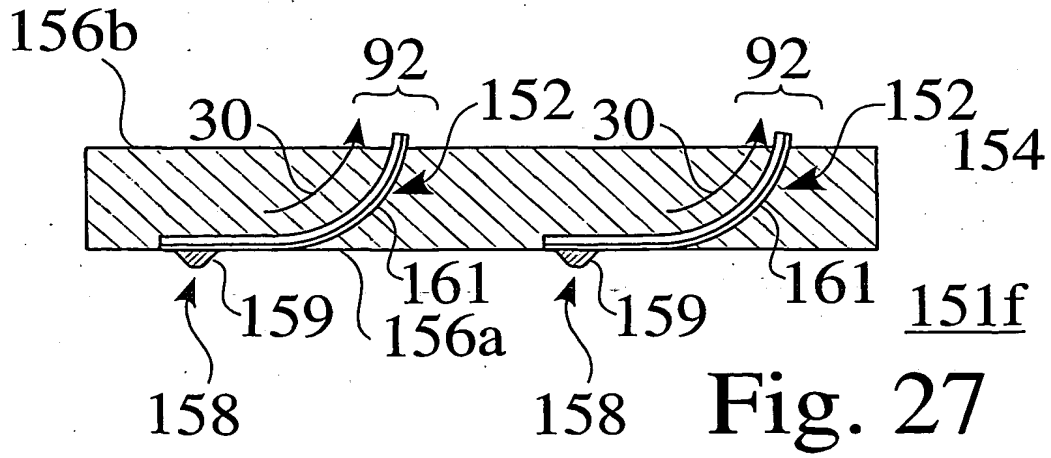


Fig. 27

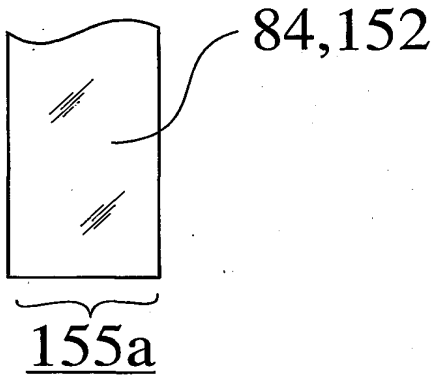


Fig. 28

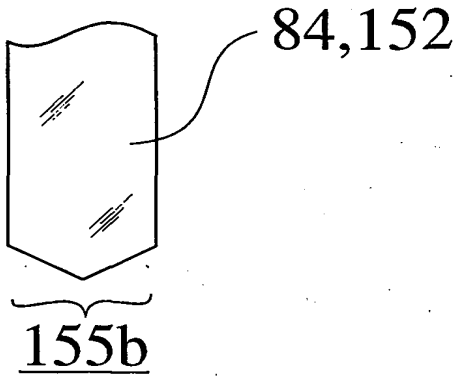


Fig. 29

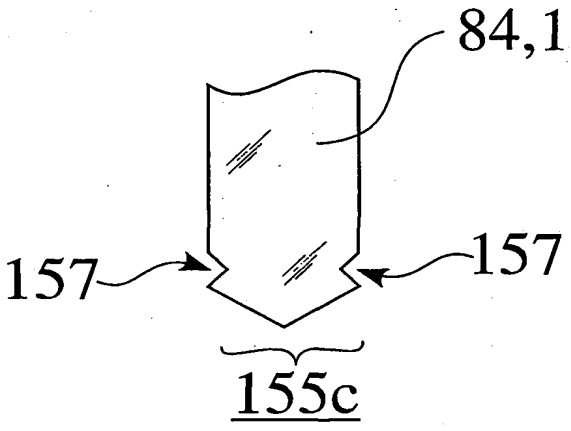


Fig. 30

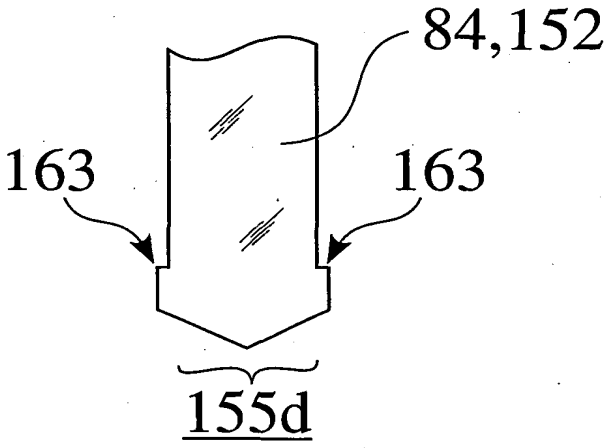


Fig. 31

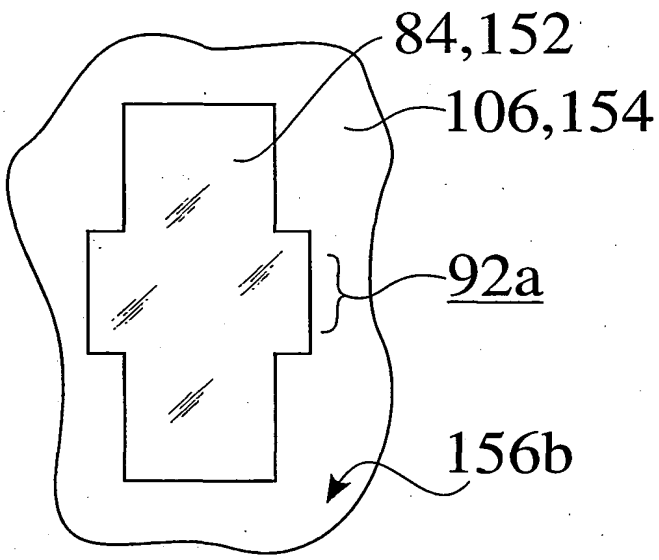


Fig. 32

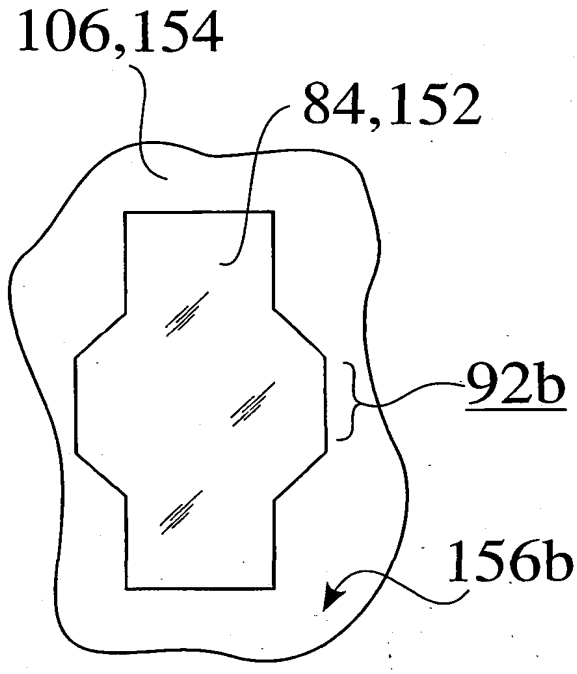


Fig. 33

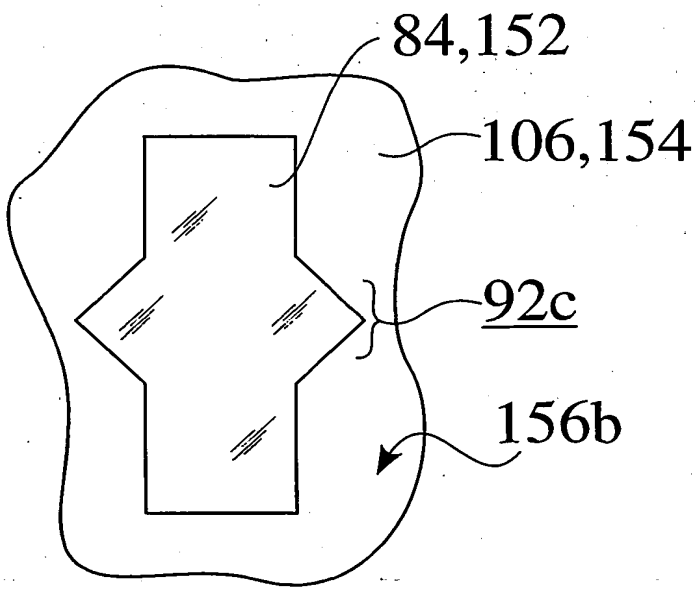


Fig. 34

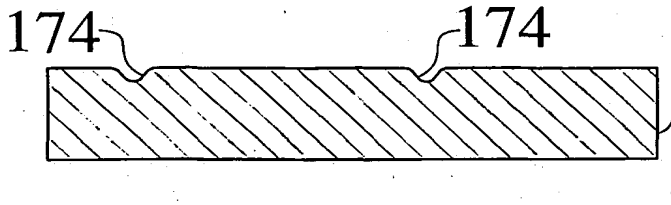


Fig. 35

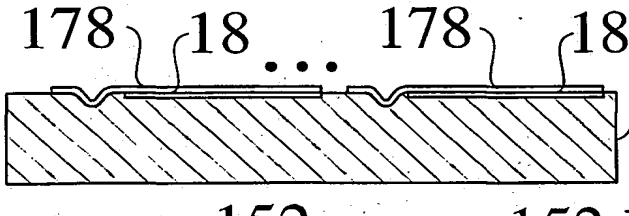


Fig. 36

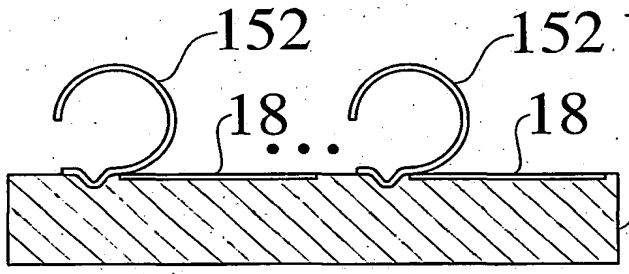


Fig. 37

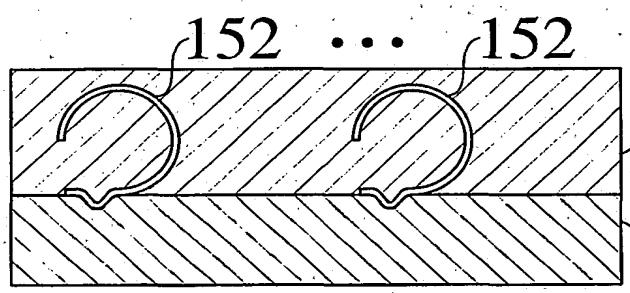


Fig. 38

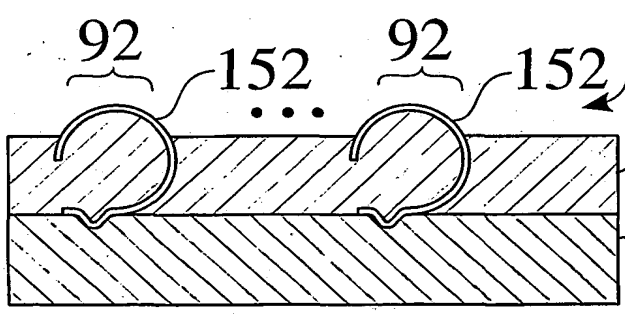


Fig. 39

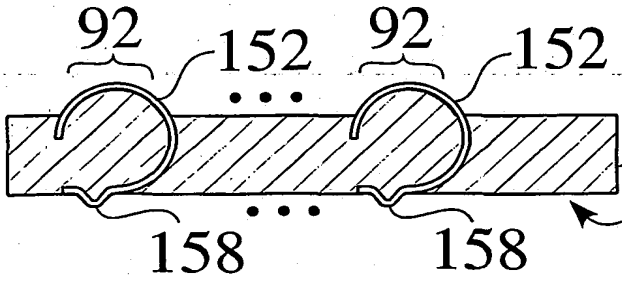


Fig. 40

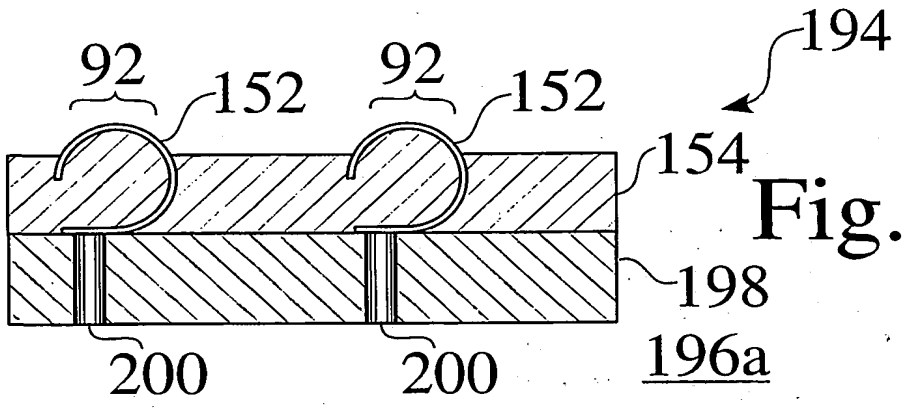


Fig. 41

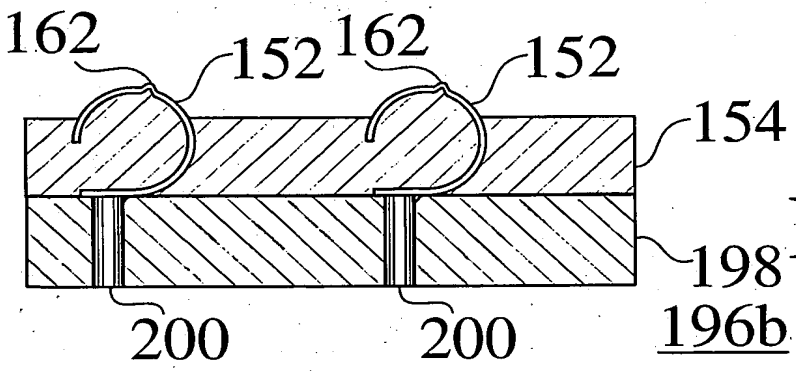


Fig. 42

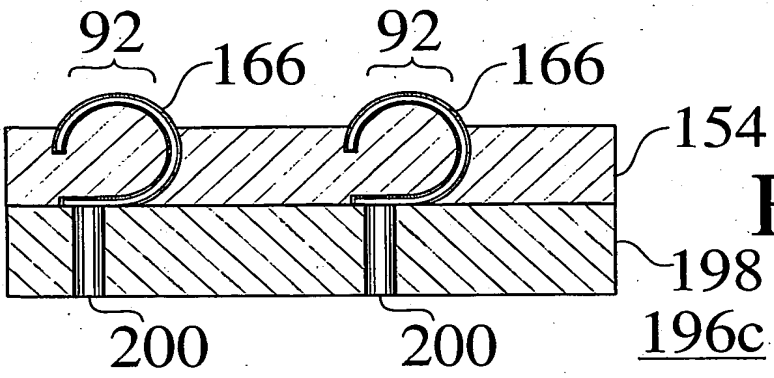


Fig. 43

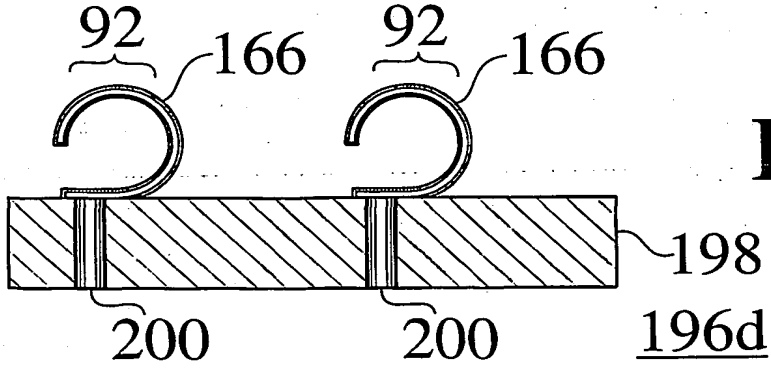


Fig. 44

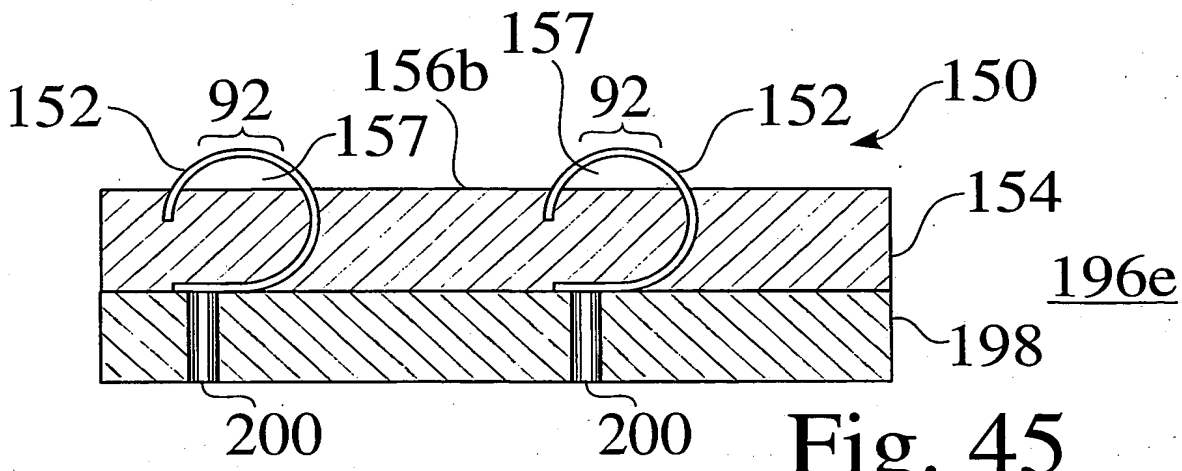


Fig. 45

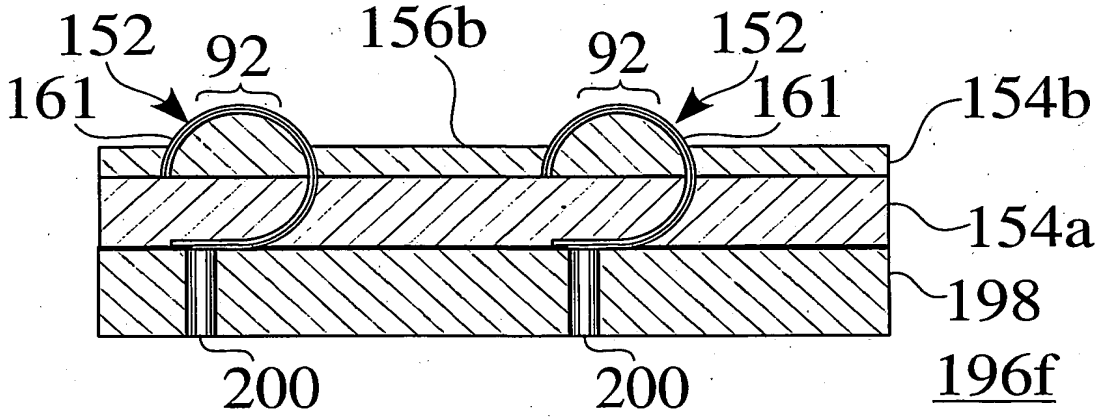


Fig. 46

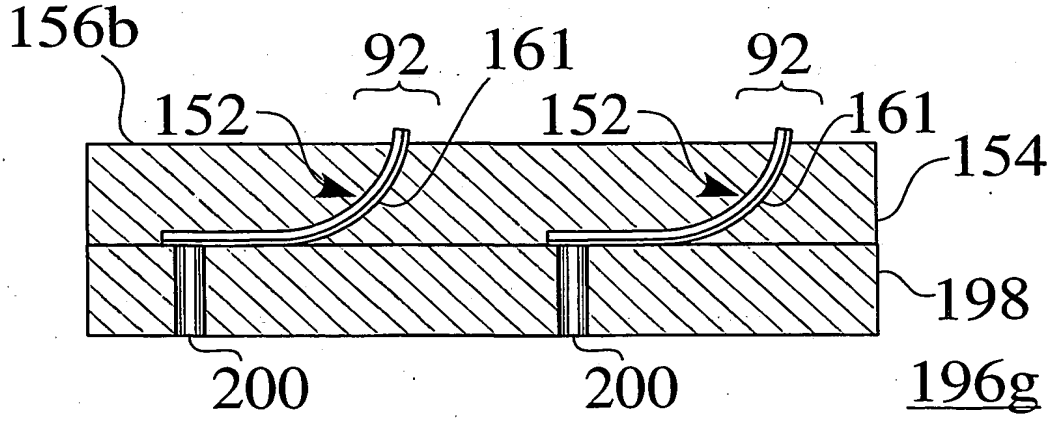


Fig. 47

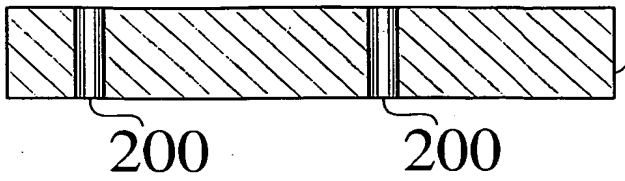


Fig. 48

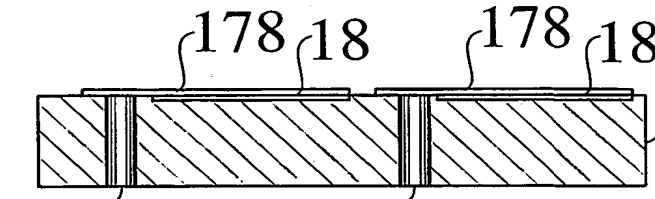


Fig. 49

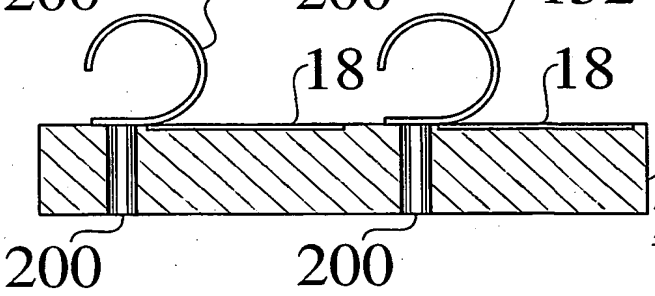


Fig. 50

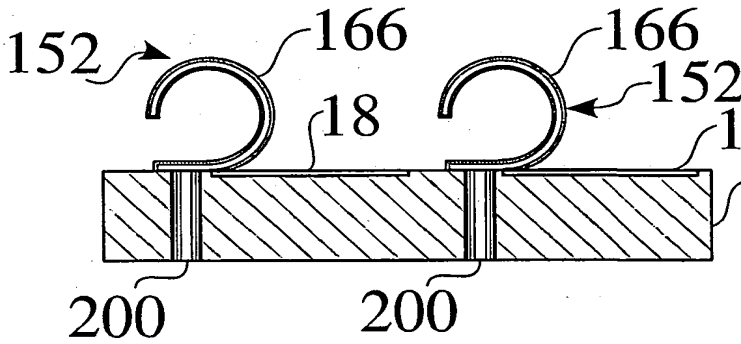


Fig. 51

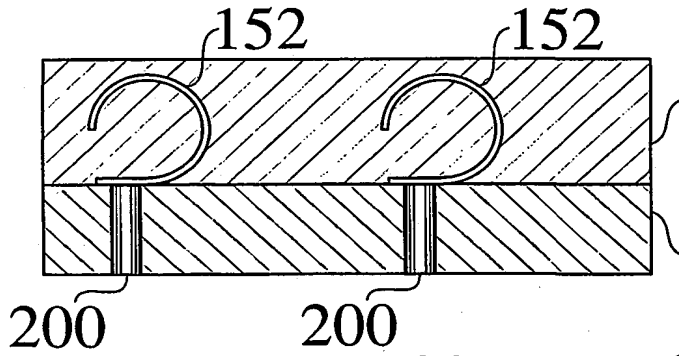


Fig. 52

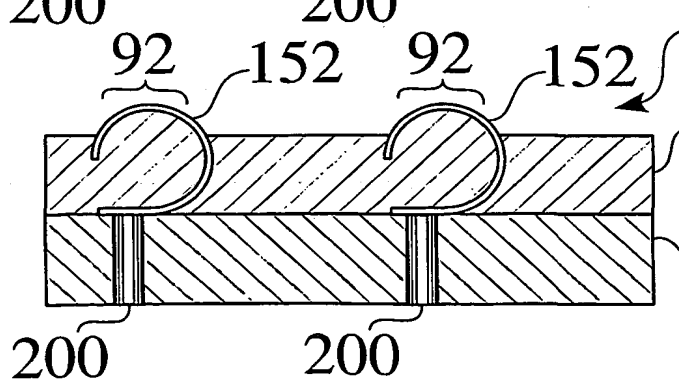


Fig. 53

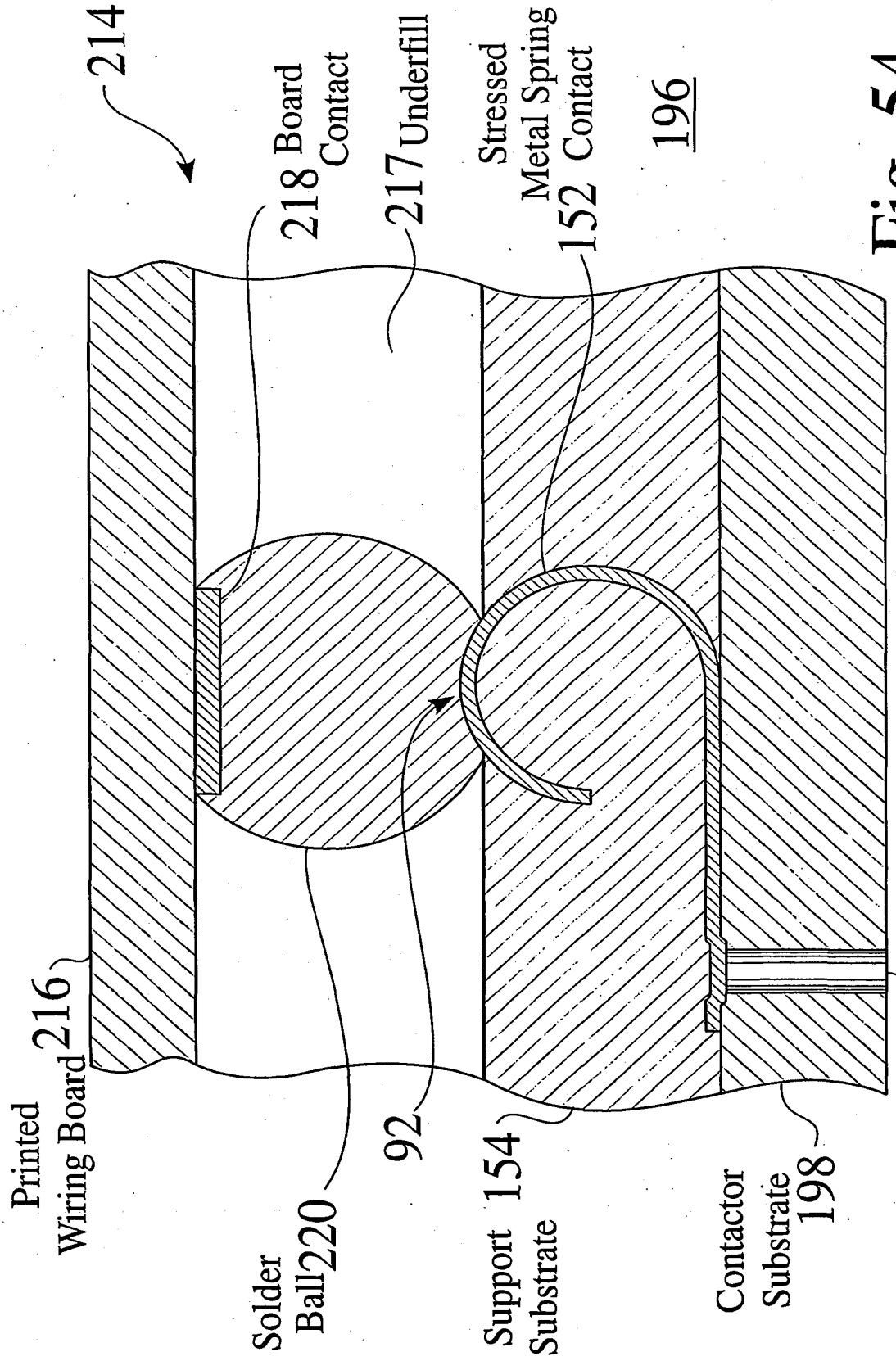
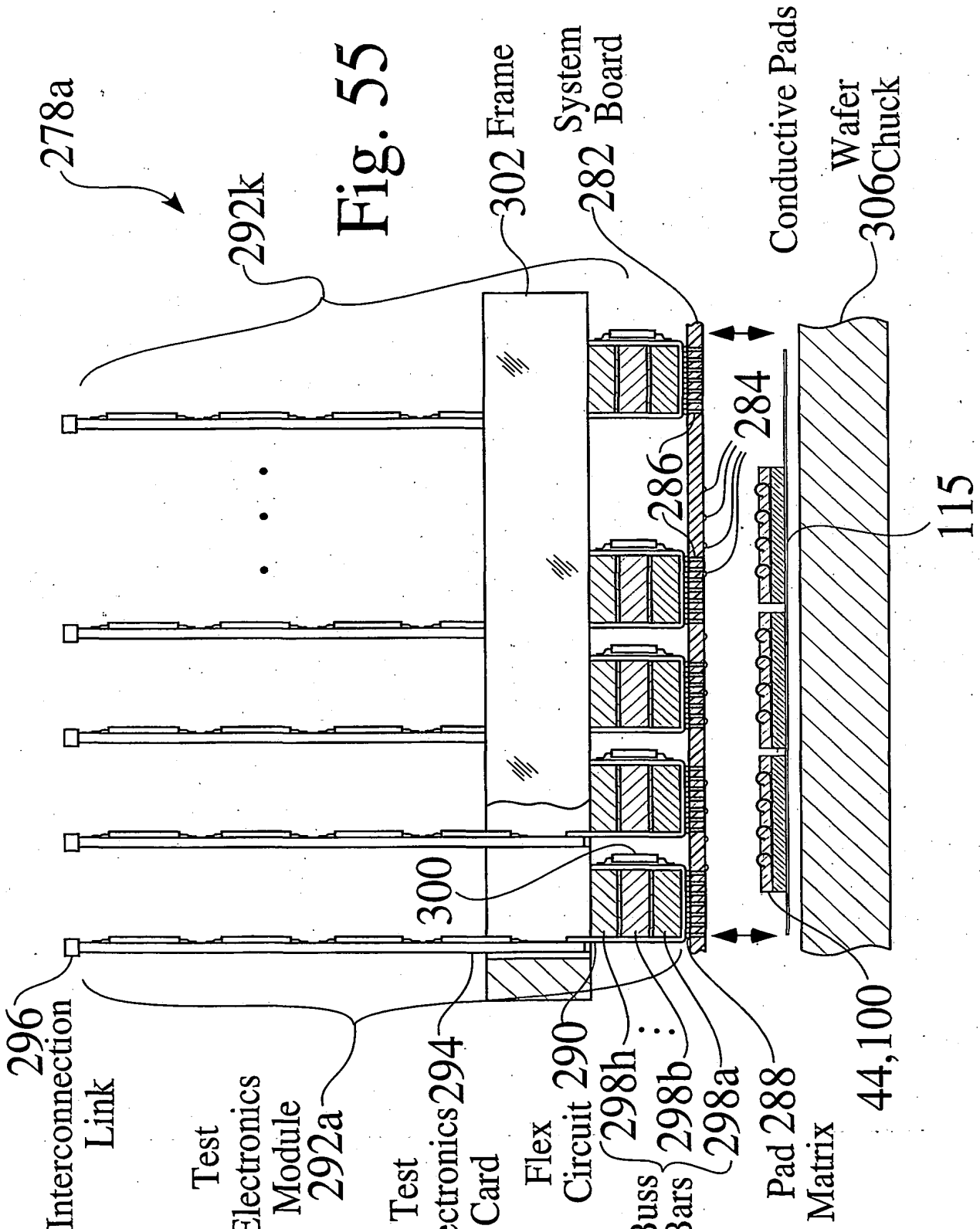

214
218 Board Contact
217 Underfill
Stressed Metal Spring 152 Contact
196
Printed Wiring Board 216
Solder Ball 220
92
Support Substrate 154
Contactor Substrate 198
200

Fig. 54

Fig. 55


278a
292k
302 Frame
282 System Board
Conductive Pads
306 Wafer Chuck
284
286
115
300
296 Interconnection Link
Test Electronics Module 292a
Test Electronics Card 294
Flex Circuit 290
Buss Bars 298h
298b
298a
Pad Matrix 288
44,100

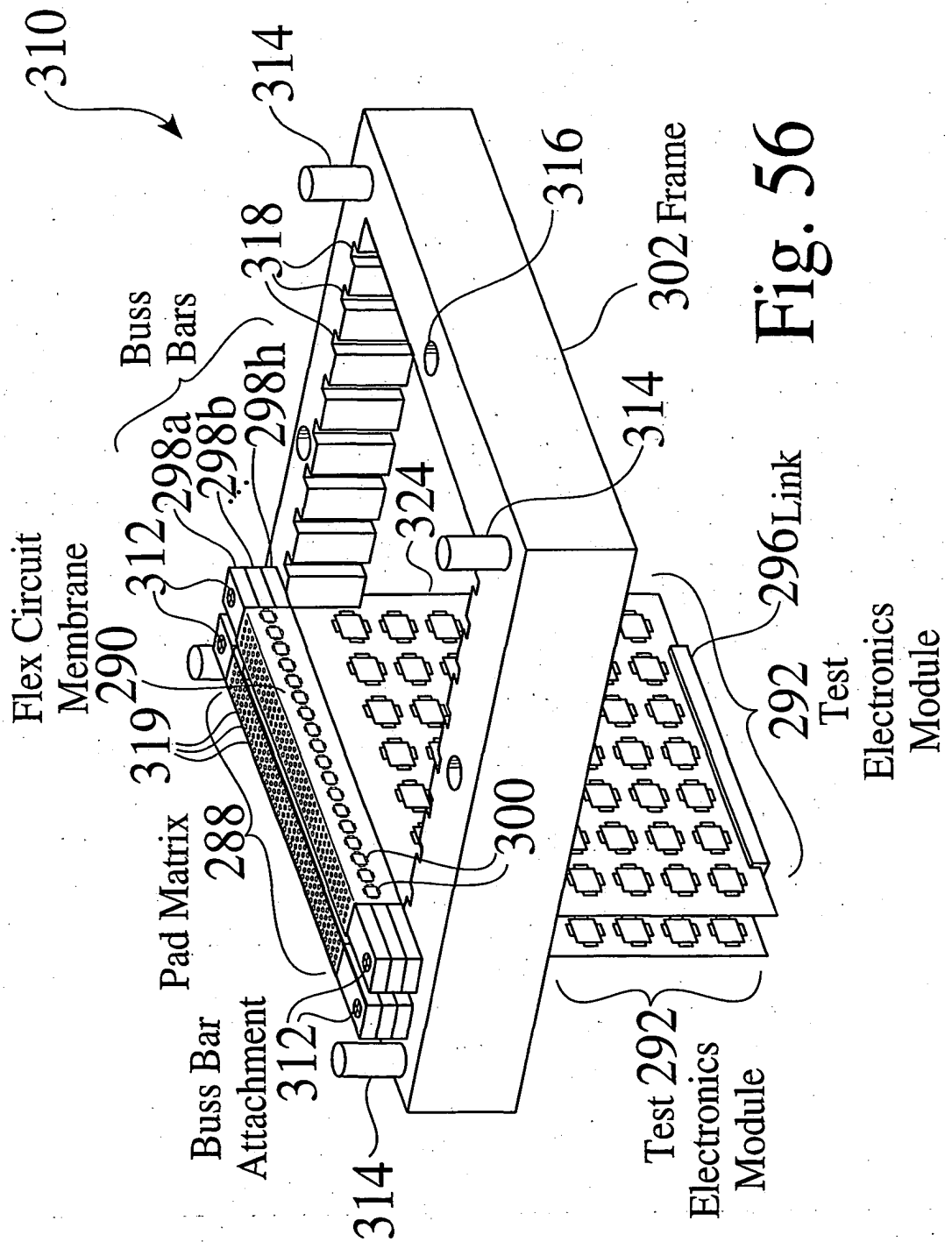
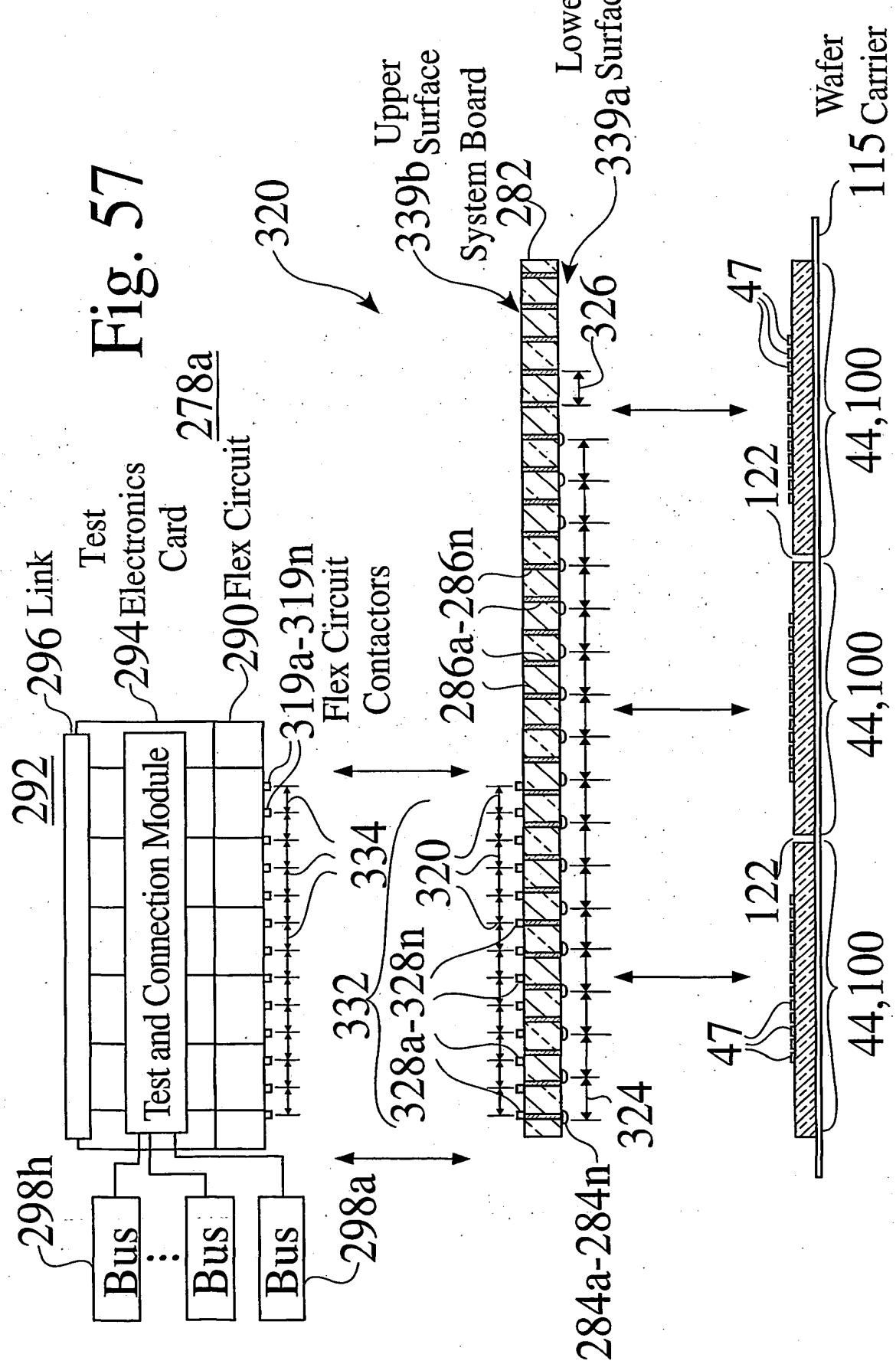

310
314
316
318
Buss Bars
298a
298b
298h
312
290
319
288
Pad Matrix
Buss Bar Attachment
312
314
Flex Circuit Membrane
324
314
302 Frame
300
296 Link
292 Test Electronics Module
Test 292 Electronics Module

Fig. 56

Fig. 57


292
296 Link
294 Test Electronics Card
290 Flex Circuit
278a
319a-319n Flex Circuit Contactors
320
339b Upper Surface System Board
282
339a Lower Surface
326
286a-286n
Test and Connection Module
334
320
332
328a-328n
324
284a-284n
298h
298a
Bus
Bus
Bus
122
47
44,100
Wafer Carrier
115

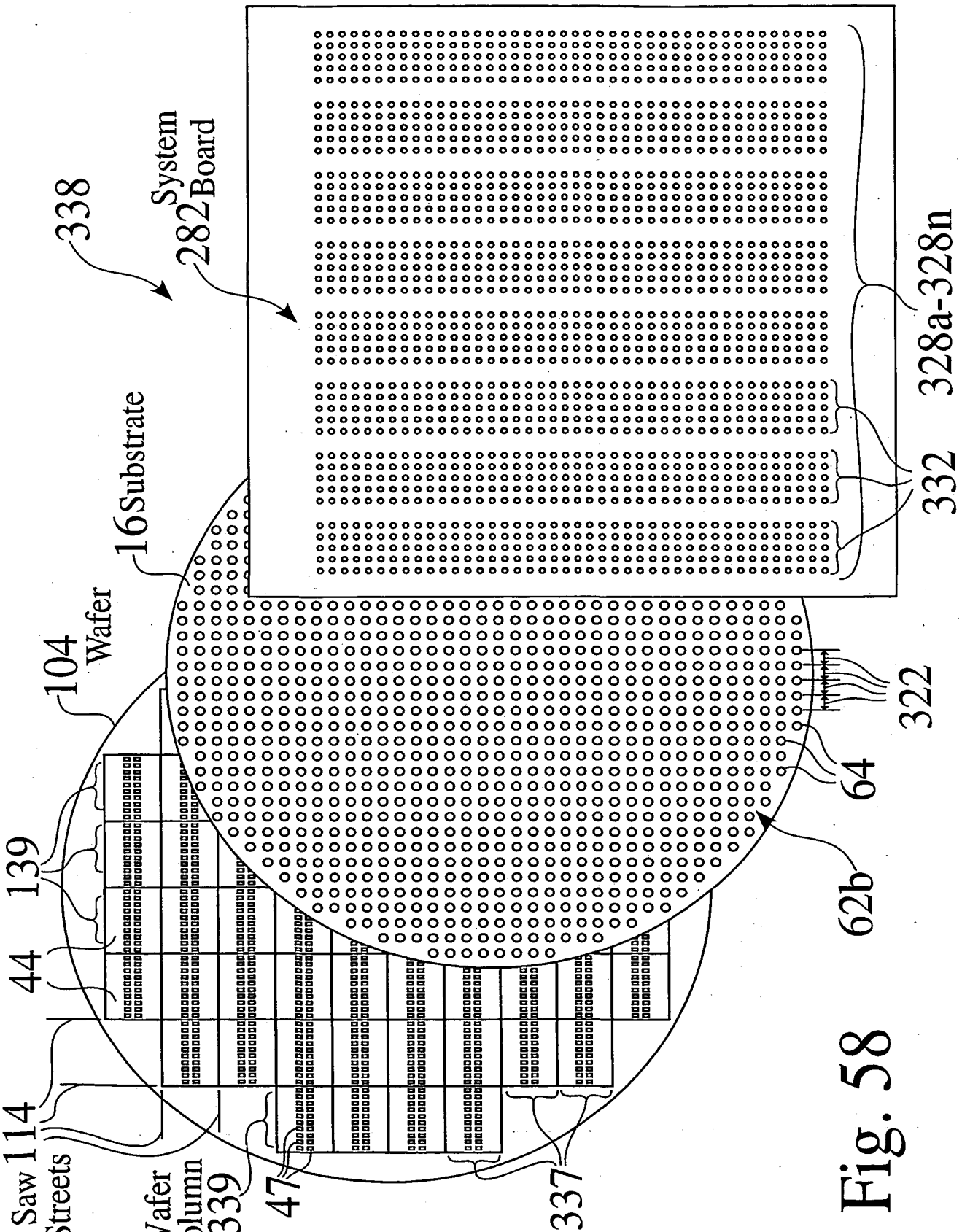

338
System
282 Board
16 Substrate
104 Wafer
328a-328n
332
322
64
62b
139
44
114
Saw
Streets
Wafer
Column
339
47
337

Fig. 58

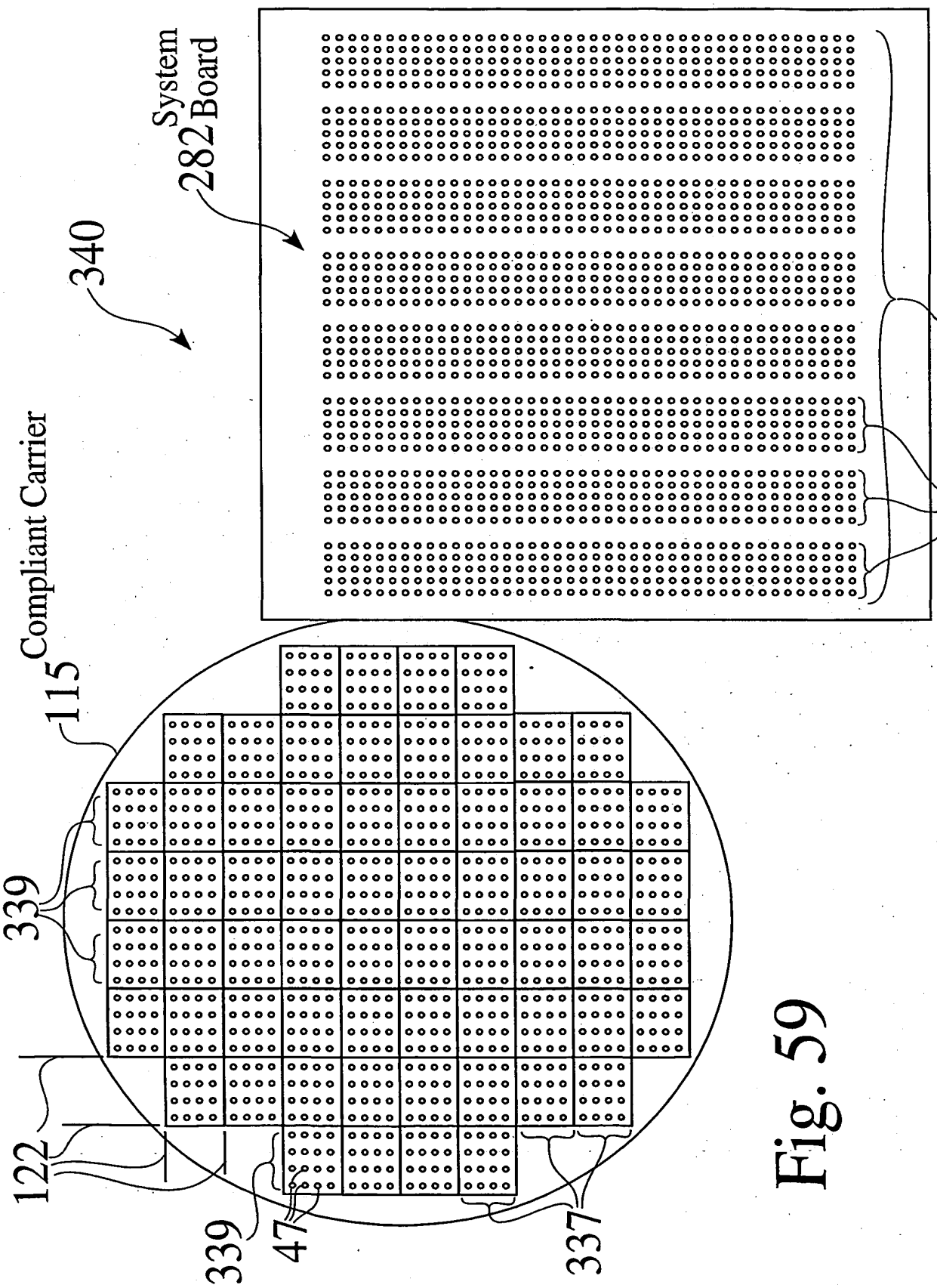

System
282 Board
340
328a-328n
332
Compliant Carrier
115
339
122
339
47
337

Fig. 59

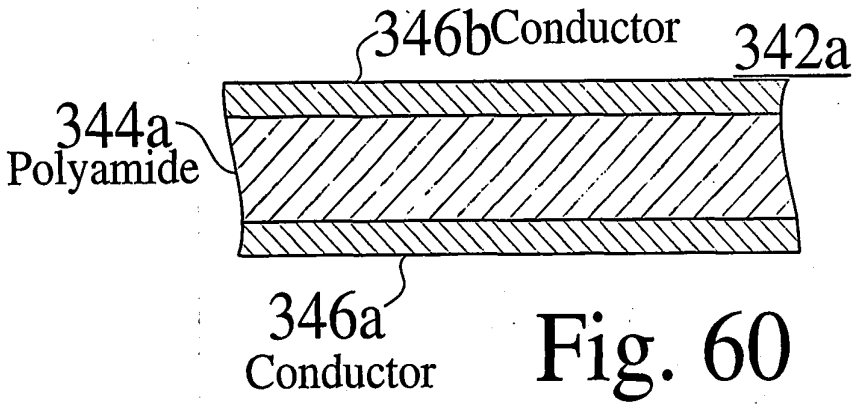


Fig. 60

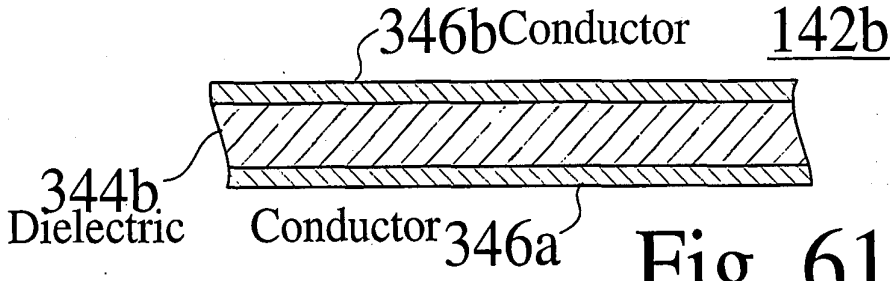


Fig. 61

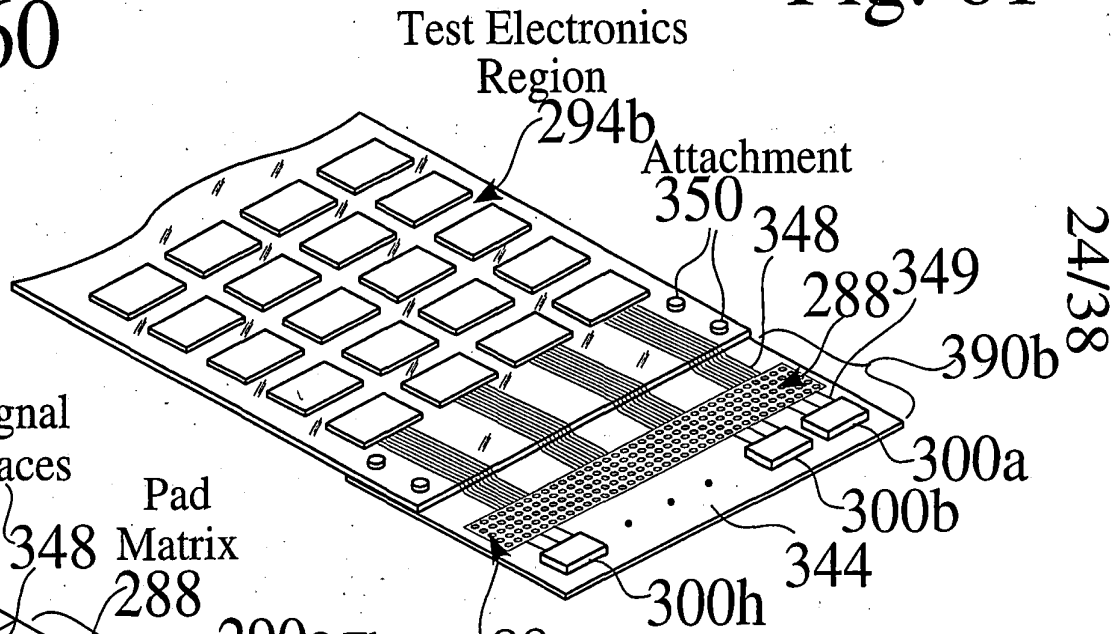


Fig. 63

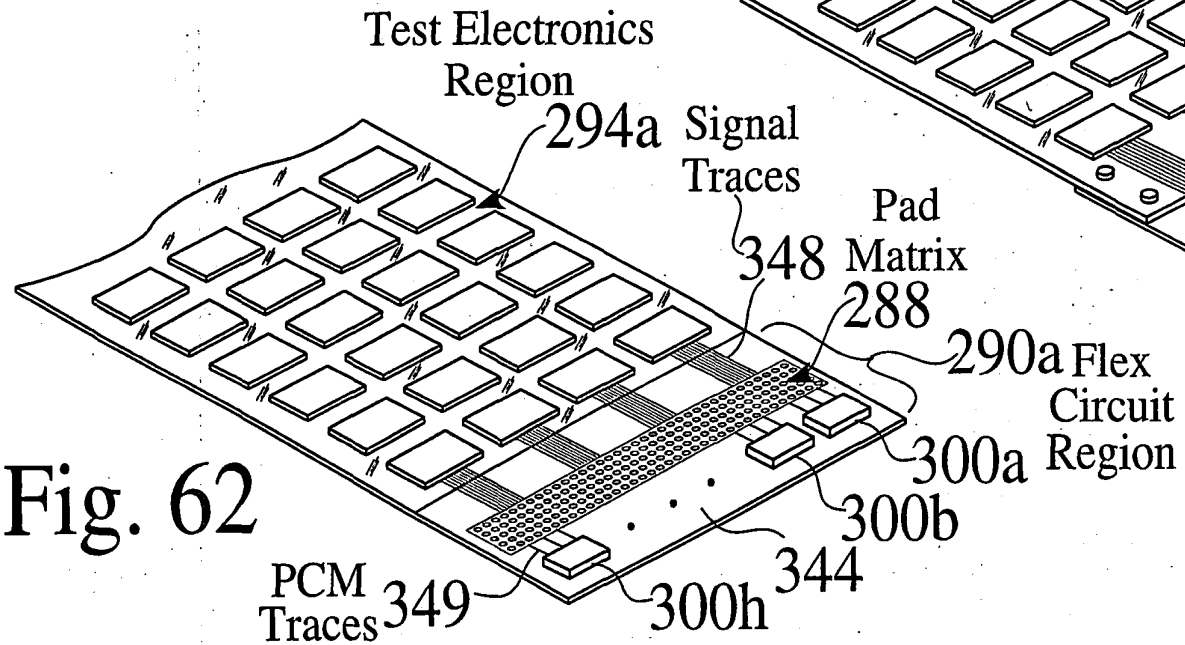


Fig. 62

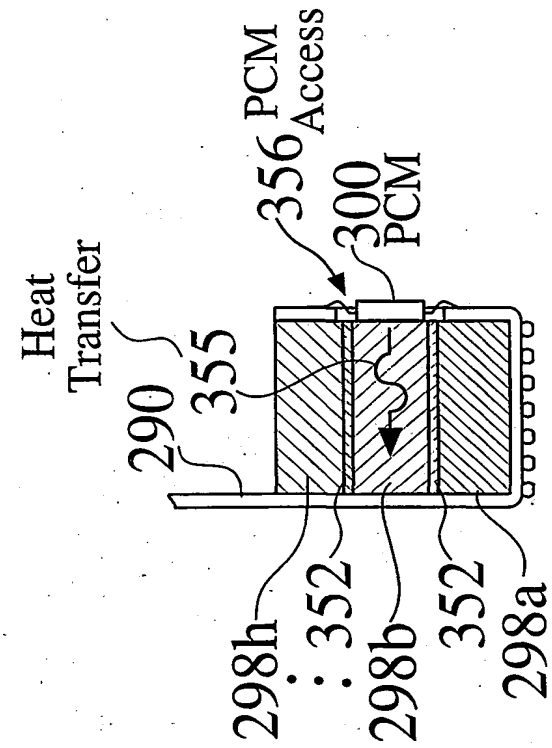


Fig. 66

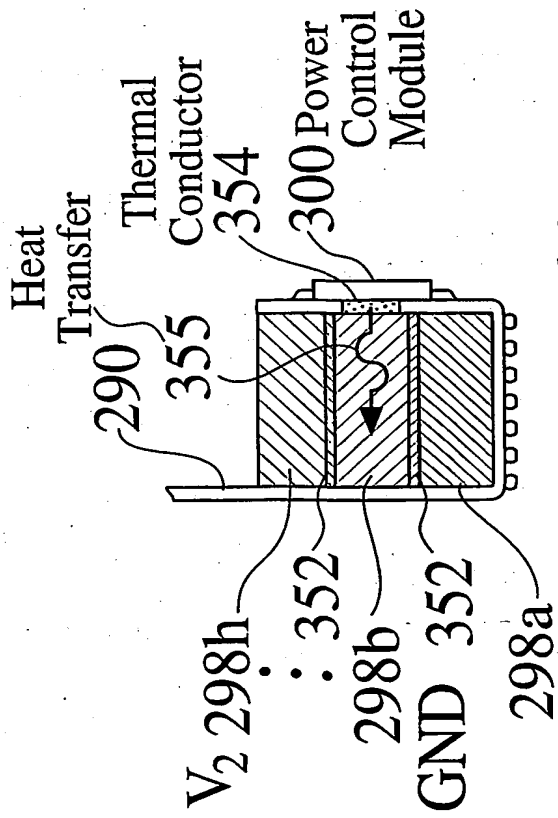


Fig. 64

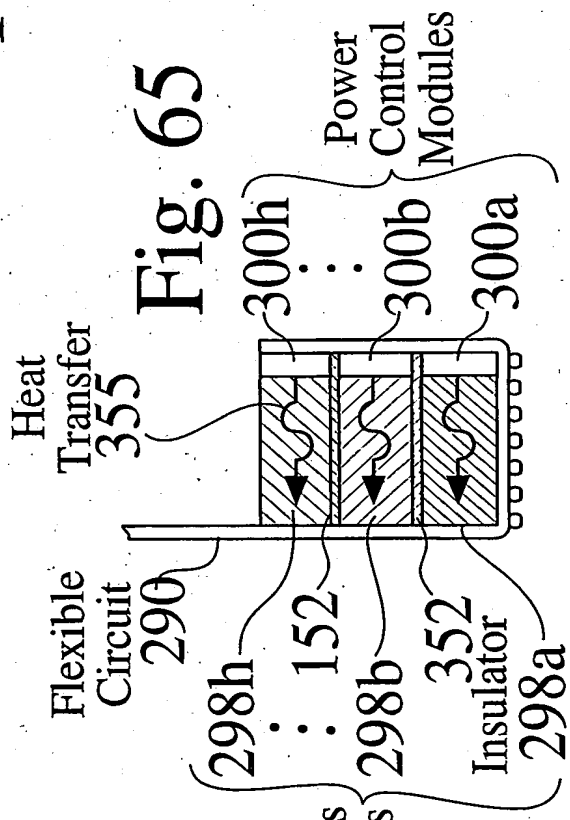


Fig. 65

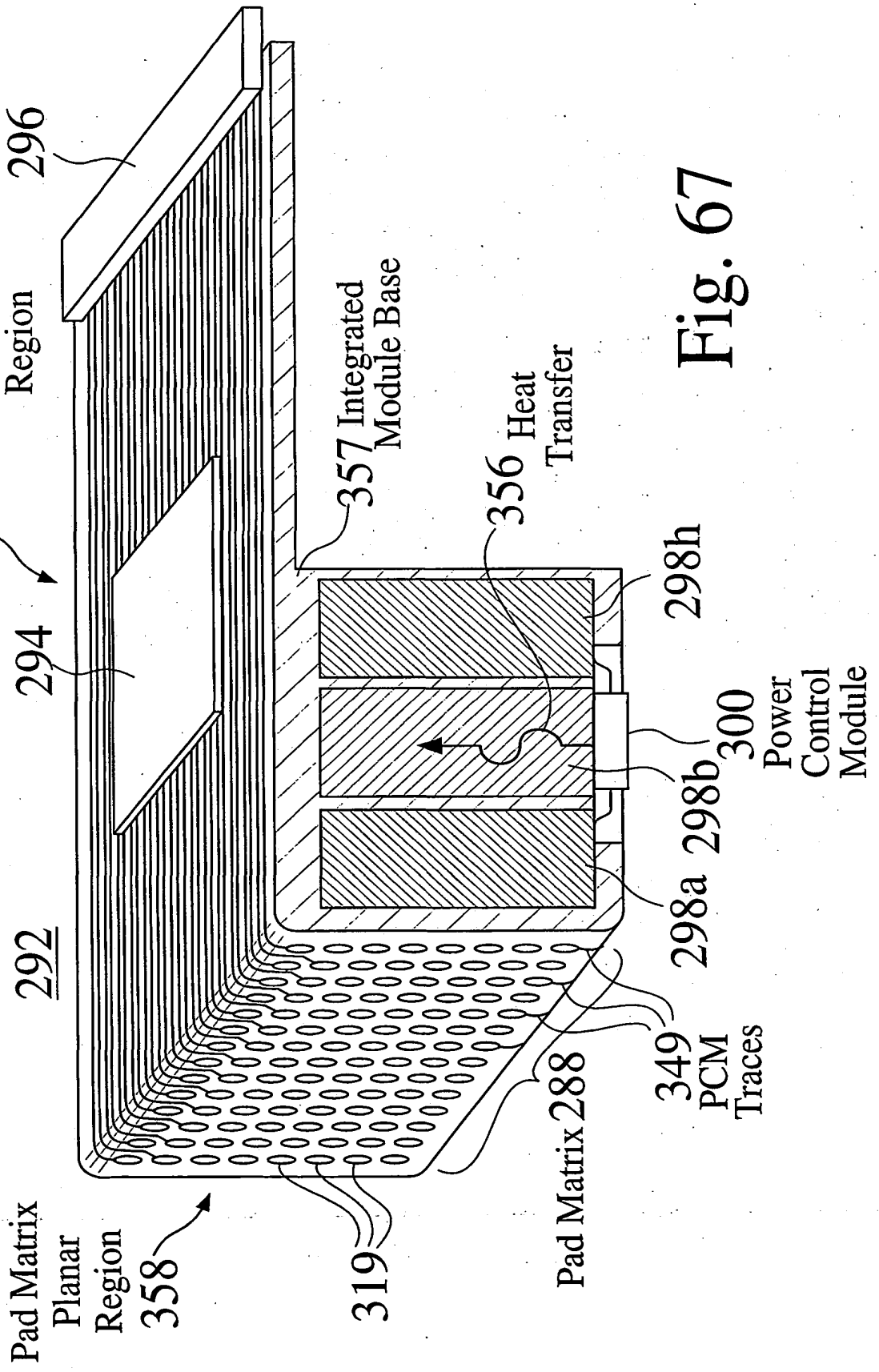

Link and Component Planar Region
359
296
294
292
357 Integrated Module Base
356 Heat Transfer
298h
300 Power Control Module
298b
298a
349 PCM Traces
Pad Matrix 288
319
Pad Matrix Planar Region 358

Fig. 67

Fig. 68

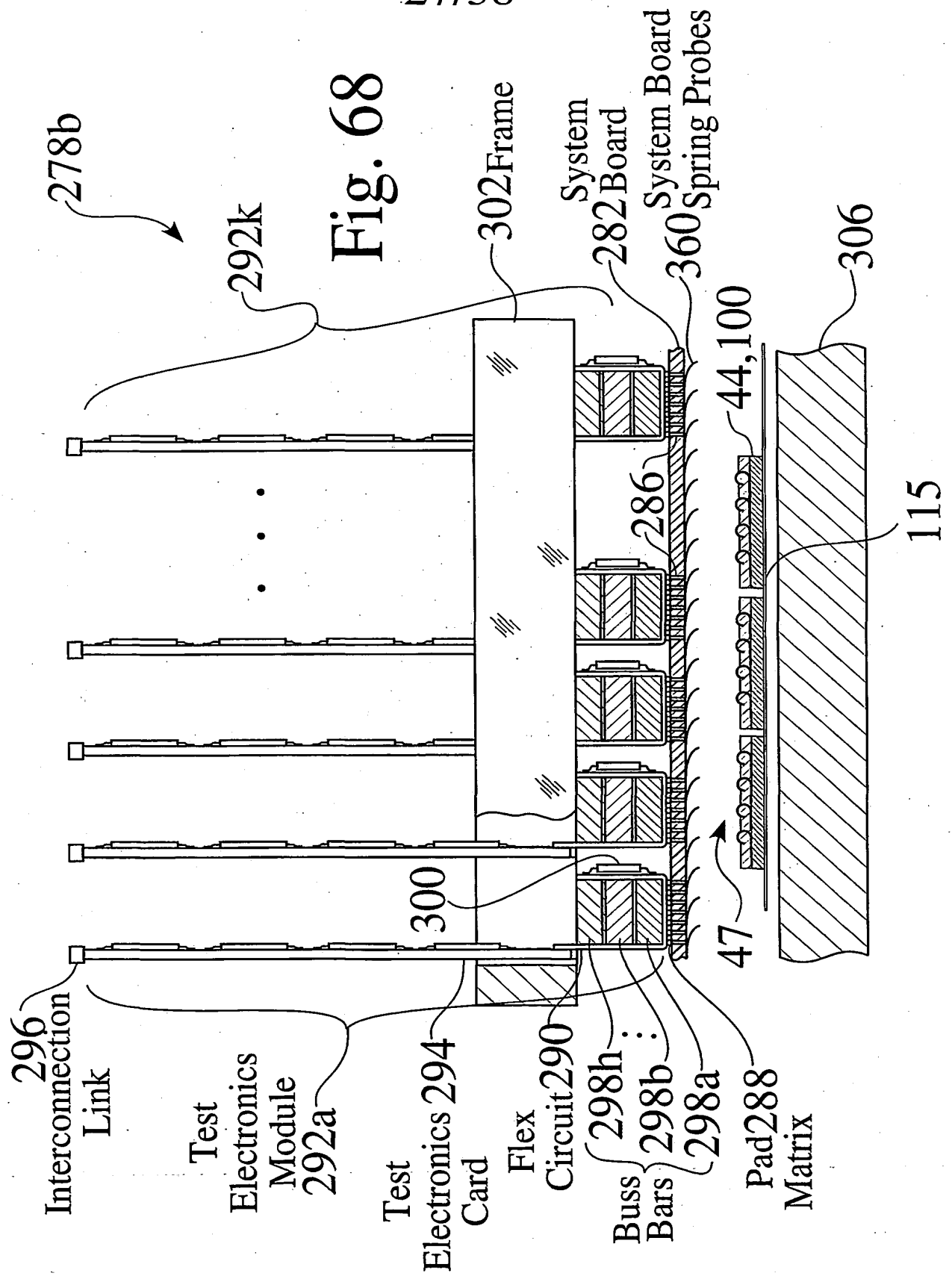

278b
292k
302 Frame
System Board 282
System Board Spring Probes 360
306
44,100
286
115
300
47
296 Interconnection Link
Test Electronics Module 292a
Test Electronics Card 294
Flex Circuit 290
298h
298b
298a
Buss Bars
Pad Matrix 288

Fig. 69

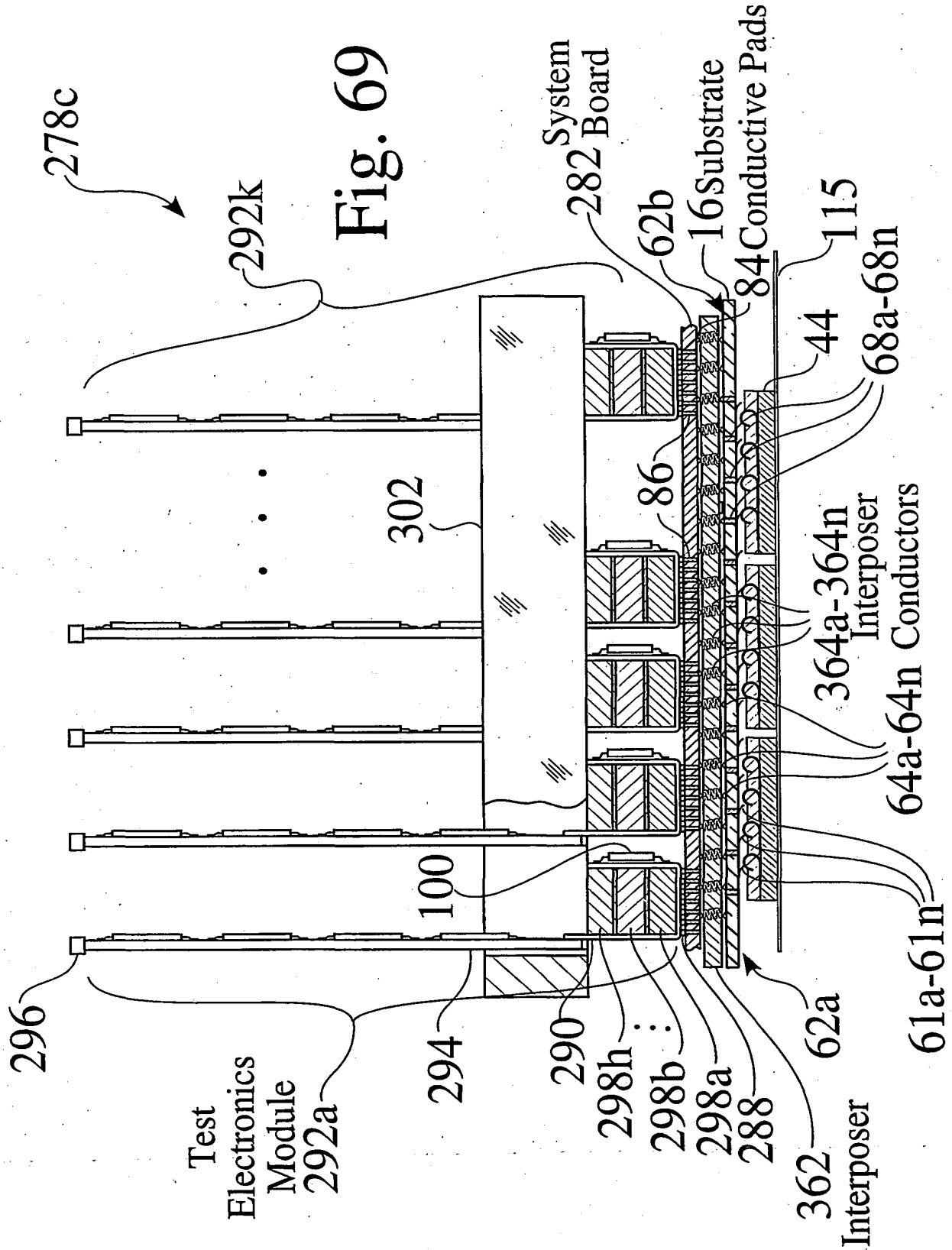

278c
292k
System Board
282
62b
16
Substrate
84
Conductive Pads
115
44
68a-68n
86
302
364a-364n
Interposer Conductors
64a-64n
100
61a-61n
296
294
290
298h
298b
298a
288
62a
362
Interposer
Test Electronics Module
292a

Fig. 70

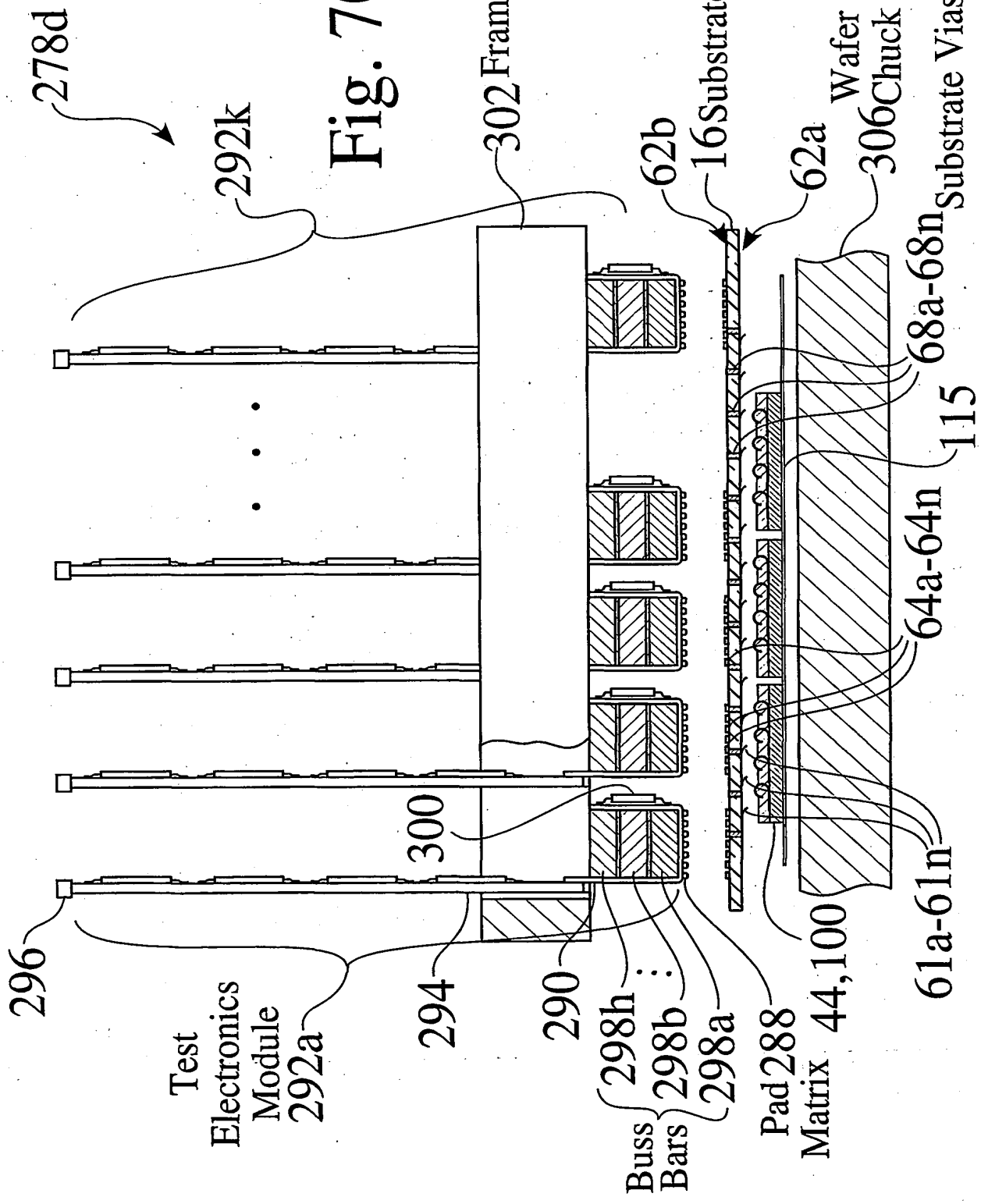

278d
292k
302 Frame
62b
16 Substrate
62a
306 Chuck
Wafer
Substrate Vias
68a-68n
115
64a-64n
61a-61n
44, 100
Pad 288
Matrix
298a
298b
298h
Buss
Bars
290
294
300
296
Test
Electronics
Module
292a

Fig. 71

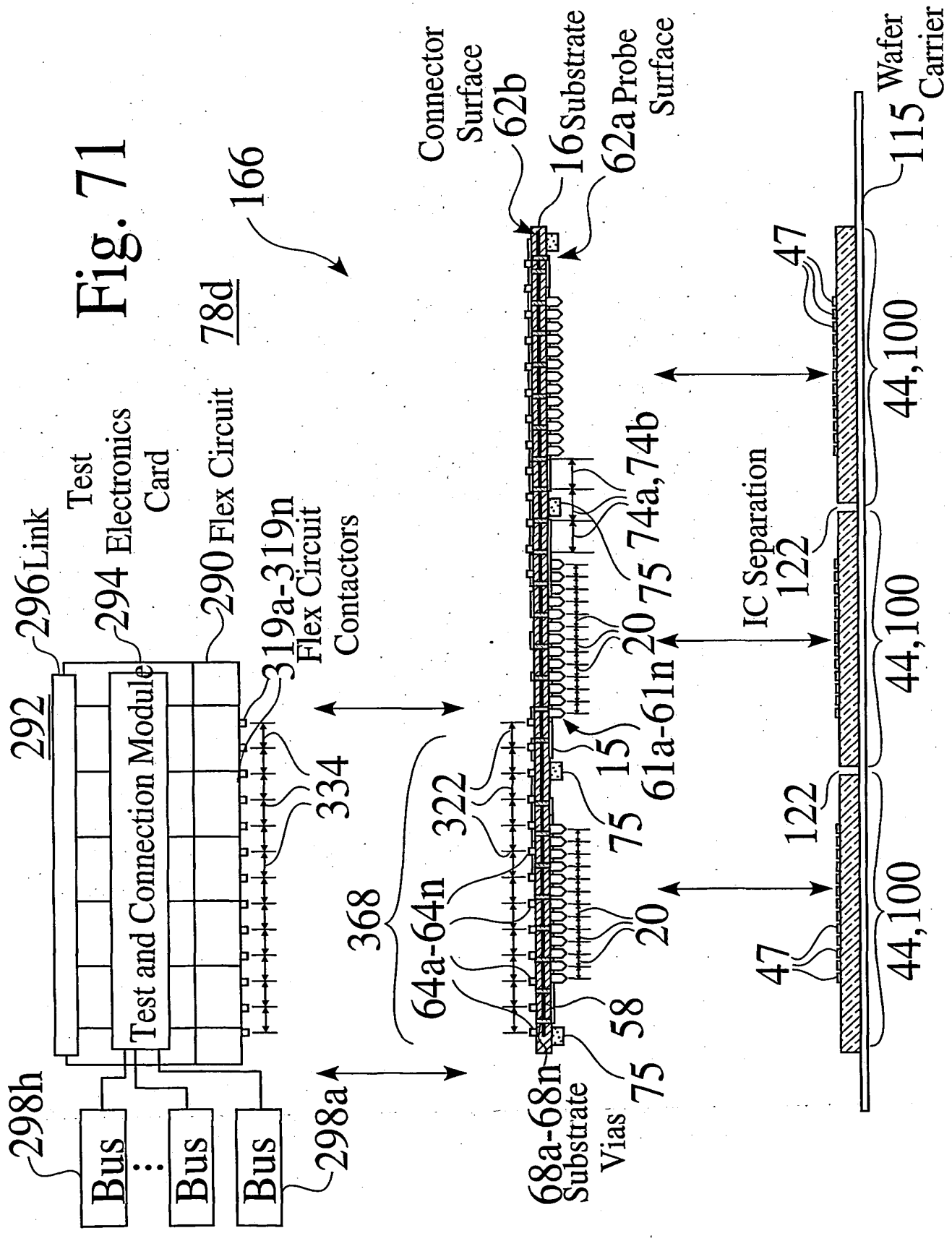
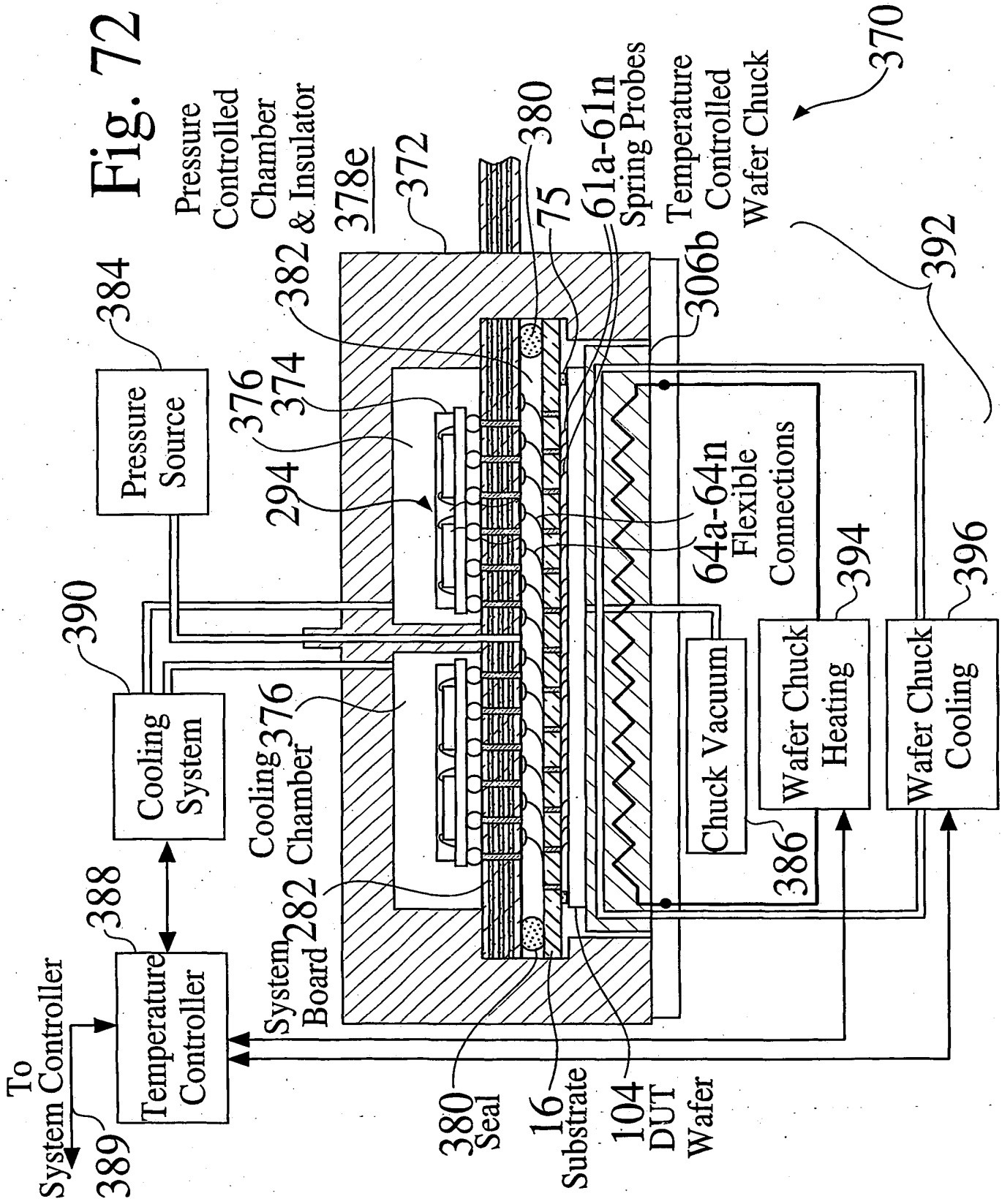

166
78d
292
296 Link
294 Test Electronics Card
290 Flex Circuit
319a-319n Flex Circuit Contactors
Test and Connection Module
Bus
Bus
Bus
298h
298a
334
322
368
64a-64n
68a-68n Substrate Vias
58
75
20
61a-61n
15
74a,74b
Connector Surface 62b
16 Substrate
62a Probe Surface
IC Separation 122
122
47
47
44,100
44,100
44,100
115 Wafer Carrier

Fig. 72


To System Controller
389
Temperature Controller
388
Cooling System
390
Pressure Source
384
Pressure Controlled Chamber & Insulator
378e
372
380
75
61a-61n Spring Probes
Temperature Controlled Wafer Chuck
370
392
306b
382
376
374
294
64a-64n Flexible Connections
394
396
Chuck Vacuum
386
Wafer Chuck Heating
Wafer Chuck Cooling
Cooling Chamber
376
System Board
282
380 Seal
16 Substrate
104 DUT Wafer

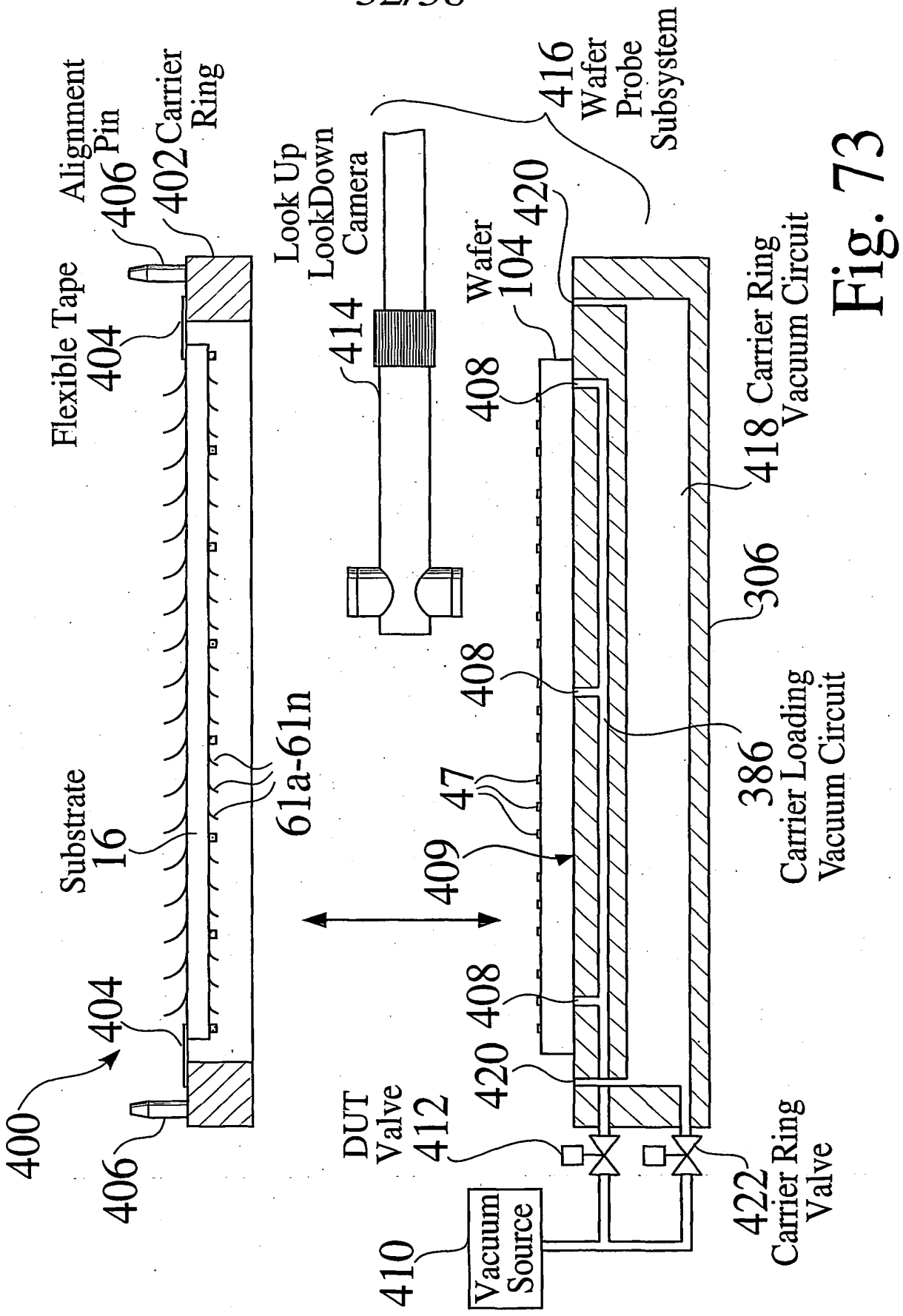

400
404
406
Flexible Tape
Alignment Pin
406
Carrier Ring
402
Substrate
16
61a-61n
Look Up LookDown Camera
414
416
Wafer Probe Subsystem
Wafer
104
420
408
418
Carrier Ring Vacuum Circuit
306
386
Carrier Loading Vacuum Circuit
47
409
DUT Valve
412
Carrier Ring Valve
422
410
Vacuum Source

Fig. 73

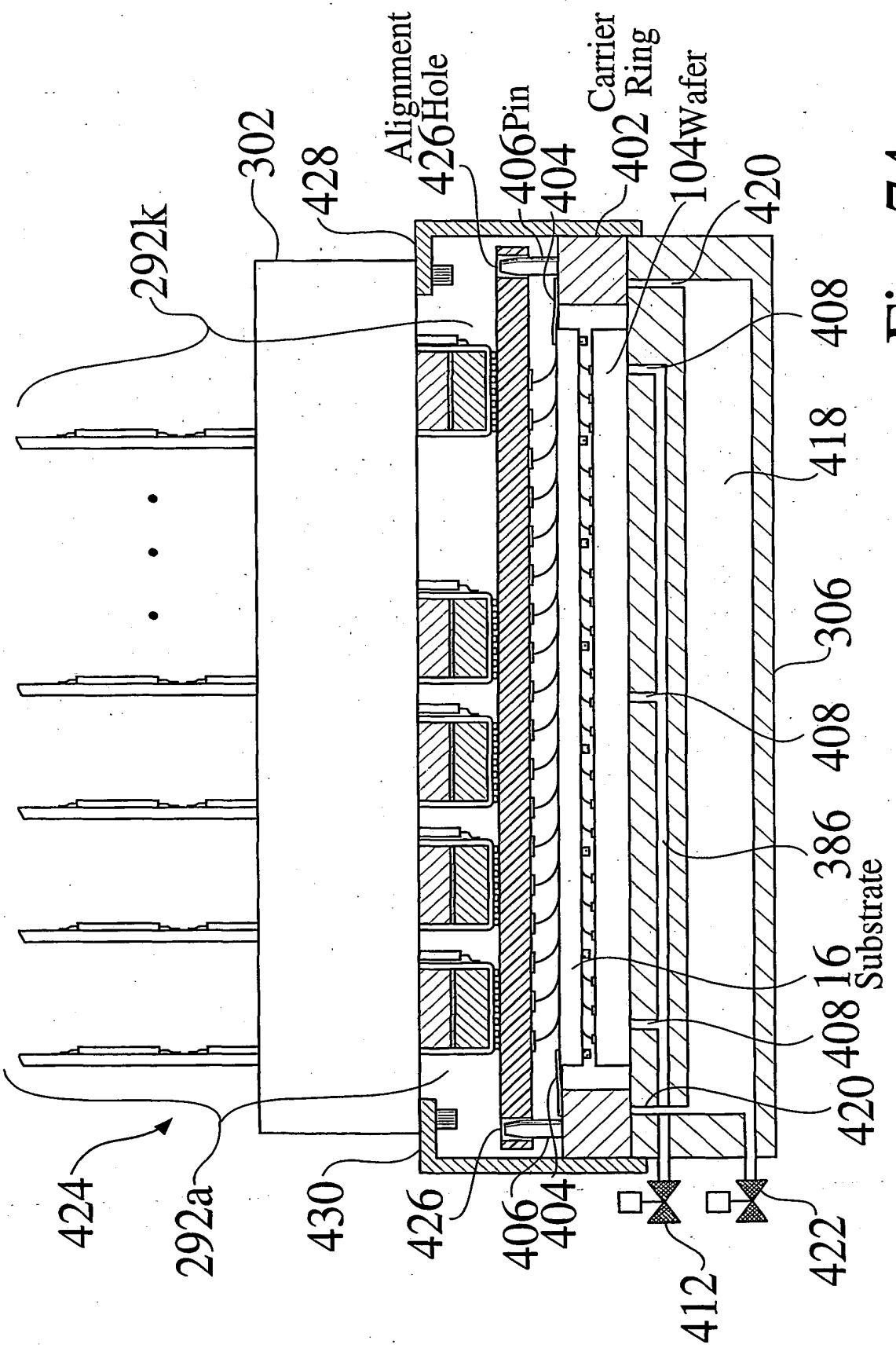

Alignment Hole 426
Pin 406
Carrier Ring 402
Wafer 104
302
428
404
420
292k
408
418
306
408
386
Substrate 16
408
420
424
292a
430
426
406
404
412
422

Fig. 74

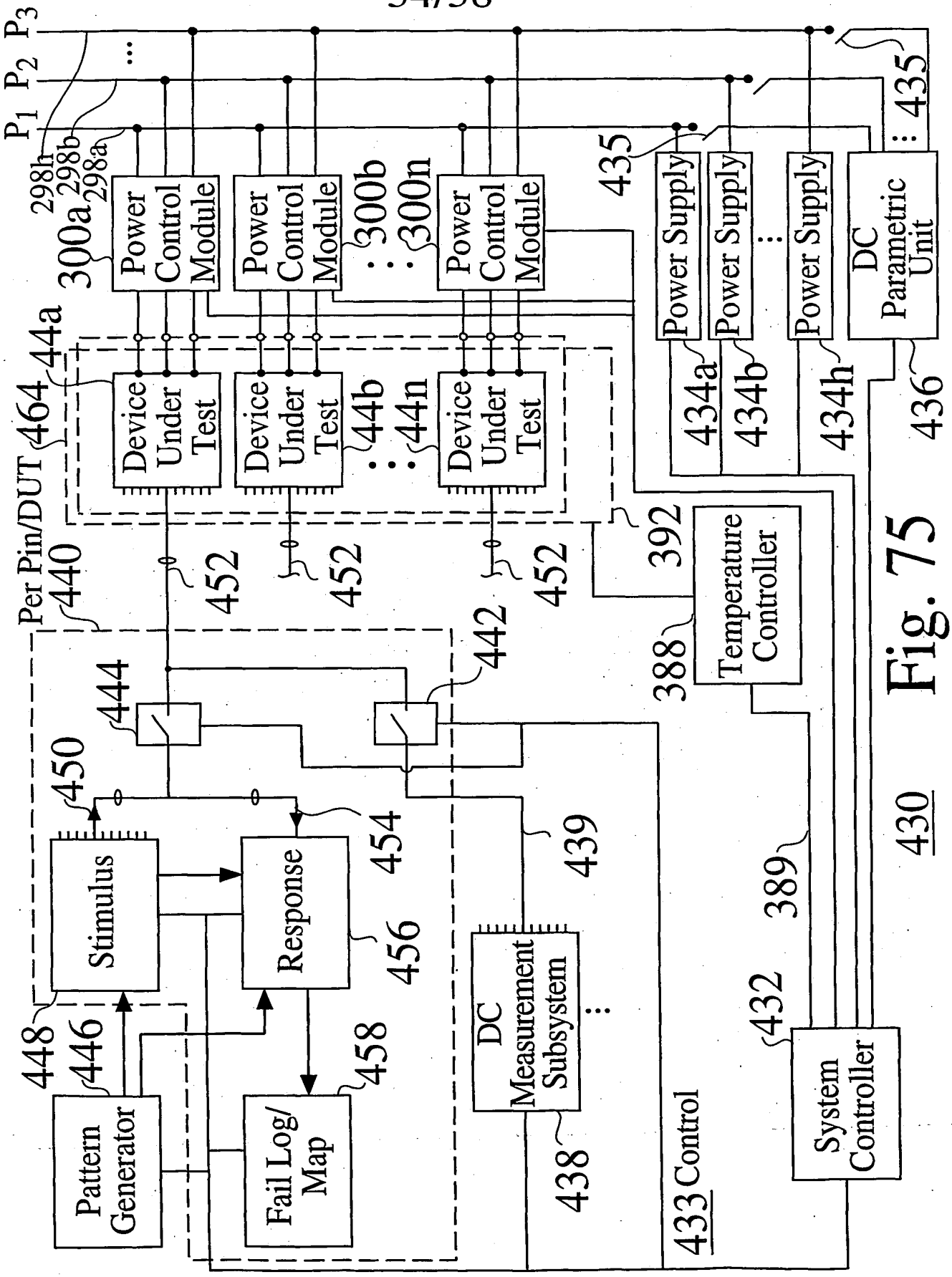

P1 P2 P3
298h 298b 298a
300a
Power Control Module
300b
300n
435
Power Supply
DC Parametric Unit
435
Device Under Test
44a 44b 44n
464
Per Pin/DUT
440
452
392
Temperature Controller
388
442
444
450
Stimulus
454
Response
456
439
448
446
Pattern Generator
458
Fail Log/ Map
DC Measurement Subsystem
438
433 Control
389
432
System Controller
430
434a 434b 434h
436

Fig. 75

Fig. 76

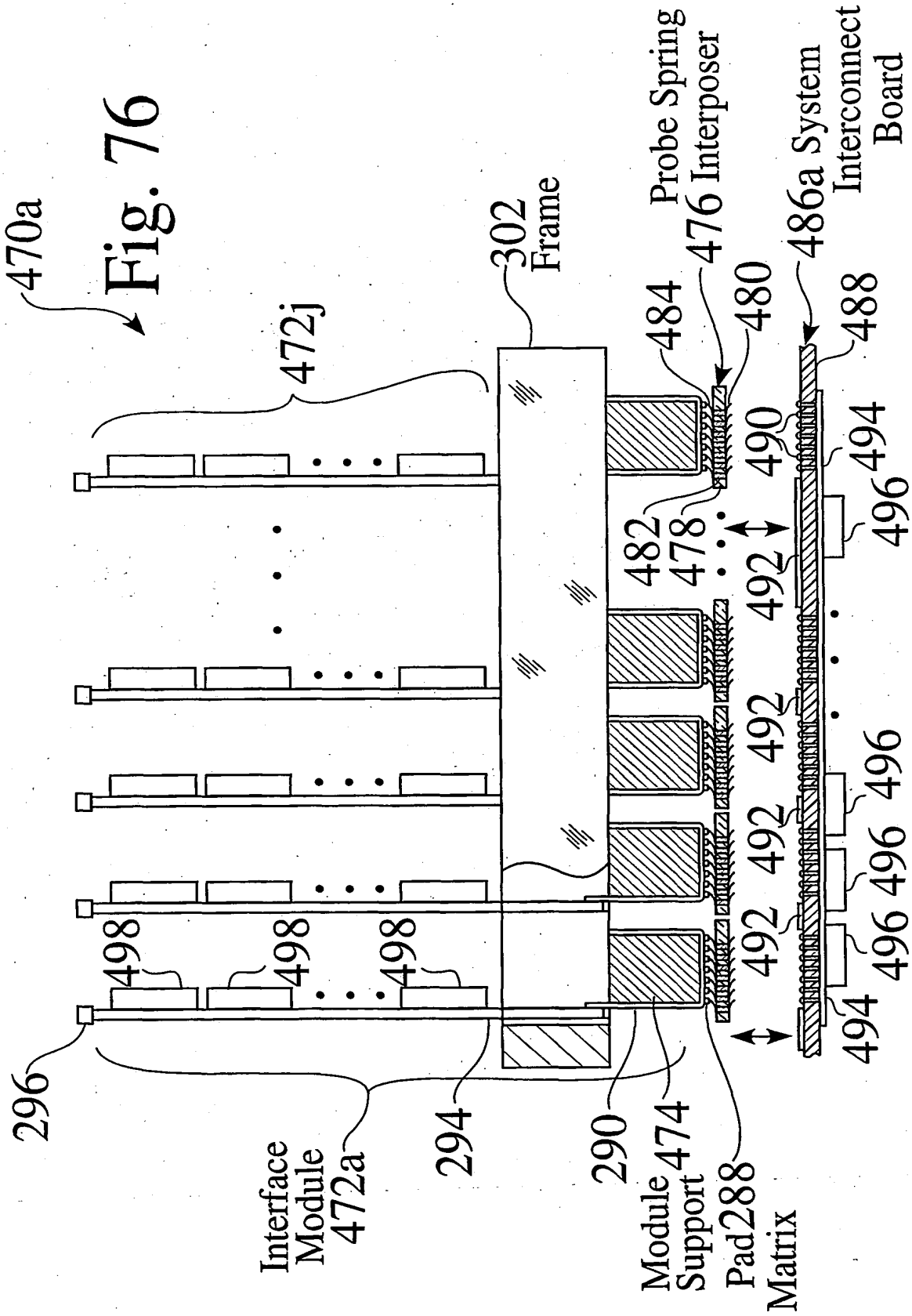
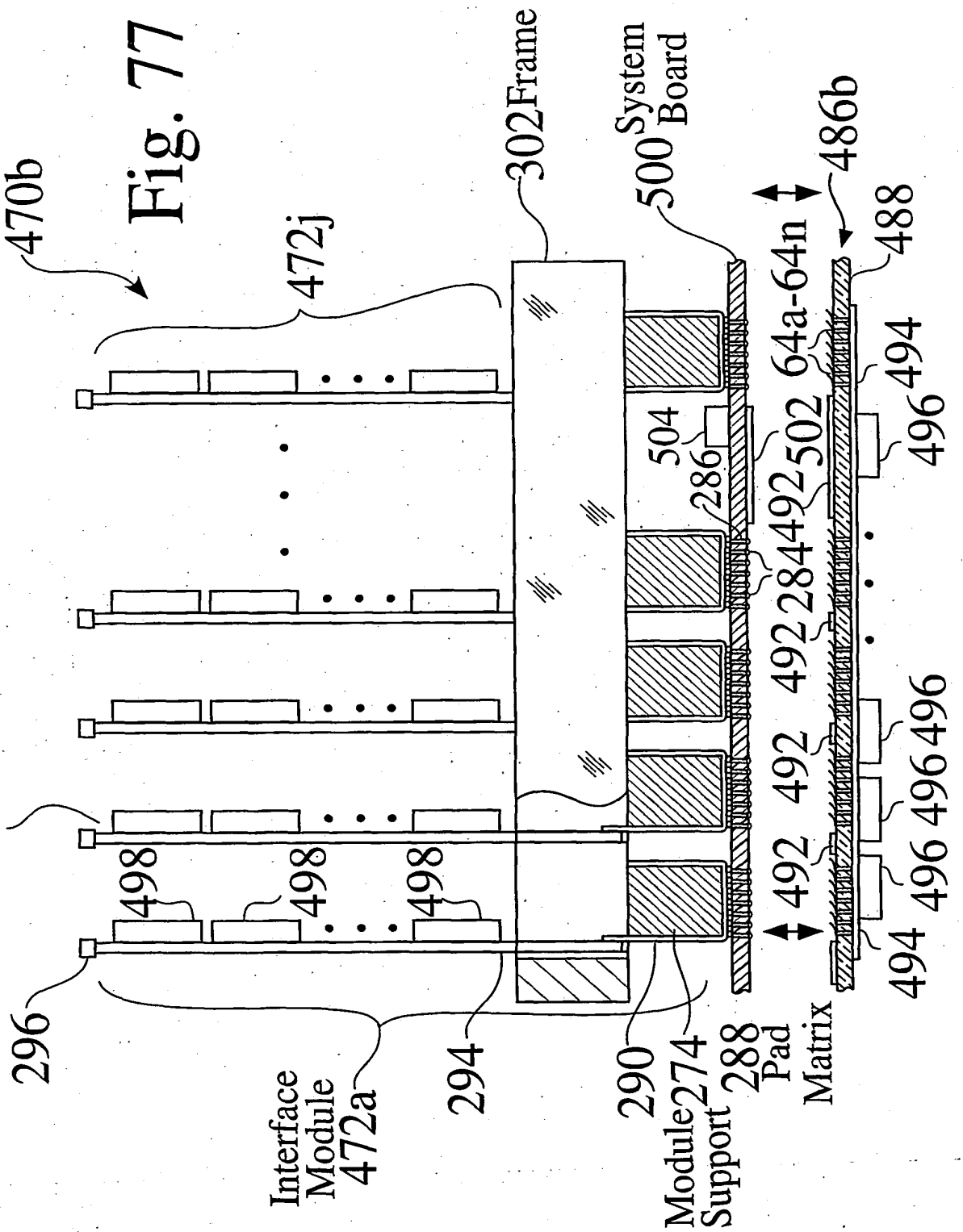

470a
472j
302
Frame
Probe Spring
476 Interposer
486a System
Interconnect
Board
484
480
488
490
494
496
482
478
492
498
296
Interface
Module
472a
294
290
Module
Support
474
Pad
Matrix
288

Fig. 77


470b
472j
302 Frame
500 System Board
486b
488
64a-64n
494
496
504
286
502
492
284
498
296
294
290
274
288
Interface Module 472a
Module Support
Pad Matrix

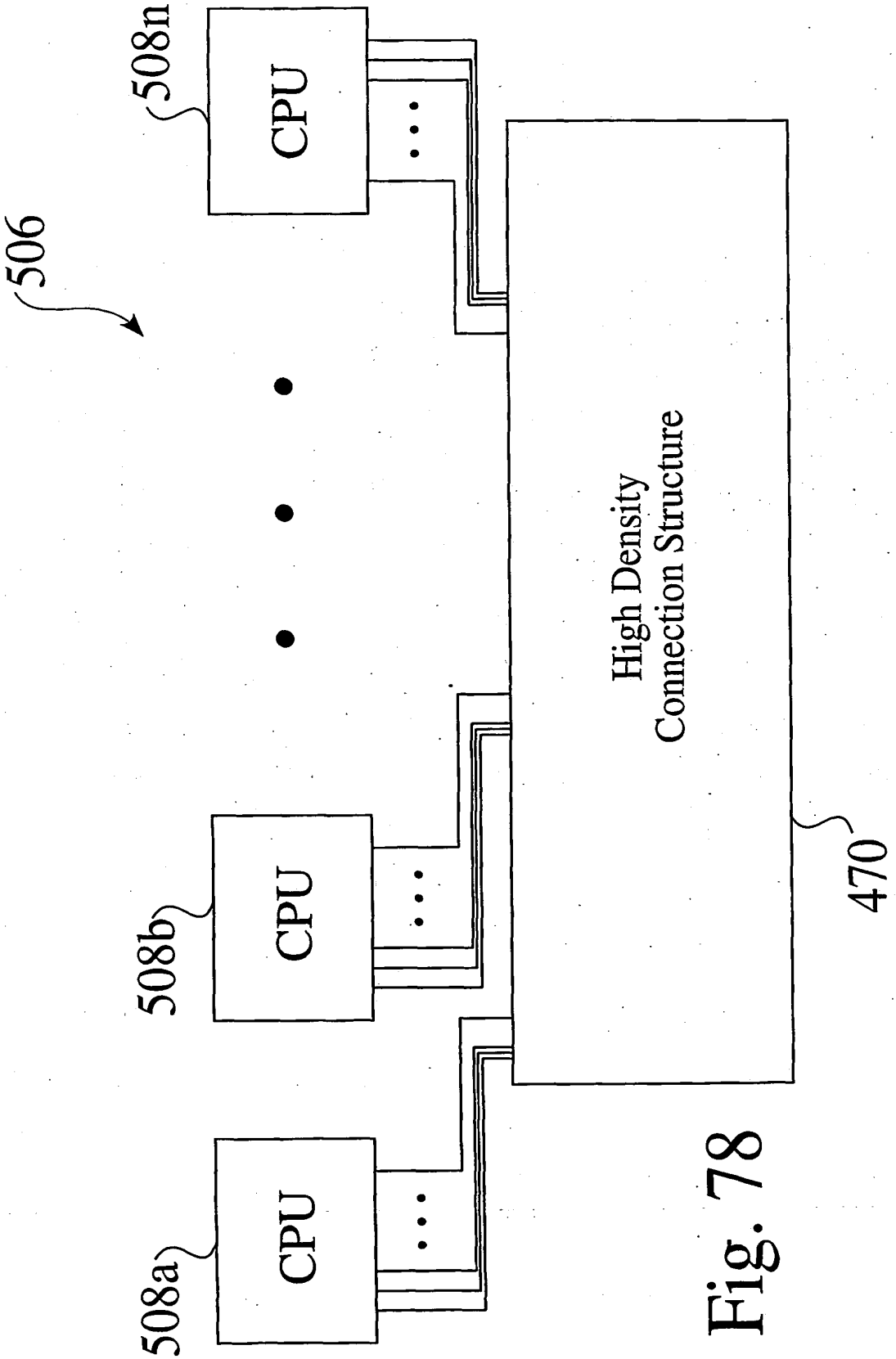

506
508n
CPU
508b
CPU
508a
CPU
High Density
Connection Structure
470

Fig. 78

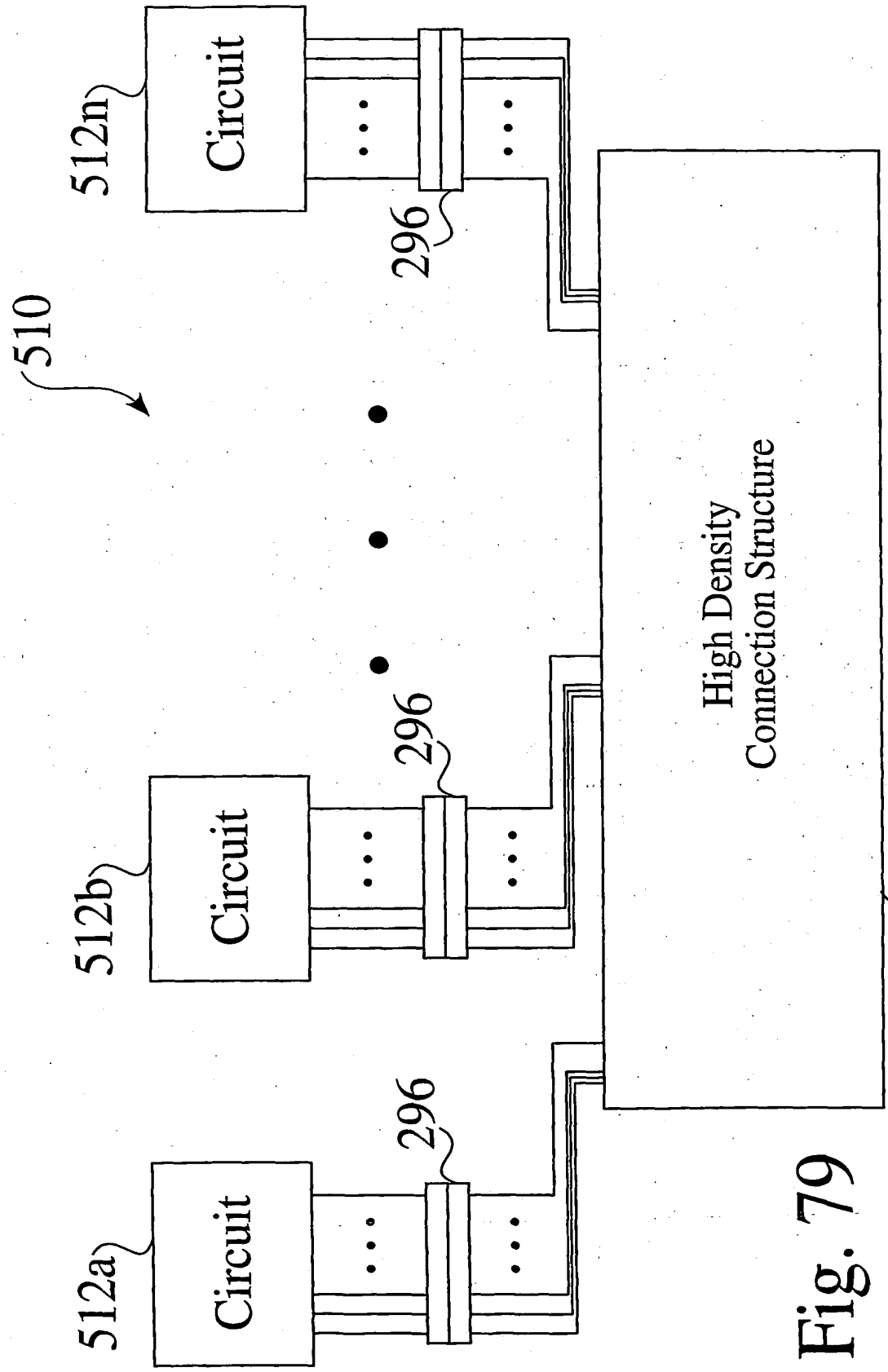

510
512a
Circuit
512b
Circuit
512n
Circuit
296
296
296
High Density
Connection Structure
470

Fig. 79